Supporting Information

Dual-port Ferroelectric NAND Flash Memory for Large Memory Window, QLC Programmable and Disturbance-Free Operations

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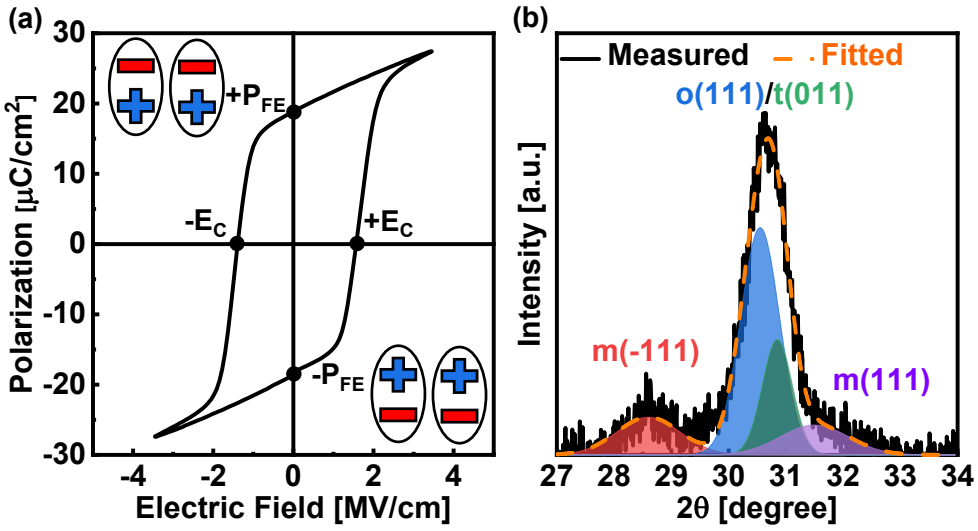

Figure S1. (a) Polarization versus electric-field curve and **(b)** XRD spectra of HZO layer after crystallization.

To characterize the ferroelectric HZO layer, polarization versus electric-field curve and XRD spectra of 10 nm thick HZO layer annealed by RTA at 600°C are measured as shown in **Figure S1a** and **S1b**. The positive and negative remnant polarization (P_{FE}) are 18.8 and -18.8 μC/cm^2, respectively. The positive and negative coercive electric-field are 1.6 and -1.4 MV/cm, respectively. The polarization values remain even after the applied bias is removed, indicating that the crystallized HZO layer has ferroelectricity.

Also, the XRD spectra show crystalline peak intensity of the monoclinic phase (m-phase), orthorhombic phase (o-phase), and tetragonal phase (t-phase). Crystallized ferroelectrics HZO typically have three phases: o-phase (ferroelectricity), t-phase (anti-ferroelectricity), and m-phase (non-ferroelectricity). To distinguish each phase, we used a Gaussian function. The peak positions for m(-111), o(111)/t(011), and m(111) are 28.6, 30.4, and 31.8, respectively[1]. The phase ratios of m(-111), o(111), t(011), and m(111) are 14.2, 52.9, 20.7, 12.2, respectively. The high o-phase ratio suggests that the crystallized HZO layer is ferroelectric.

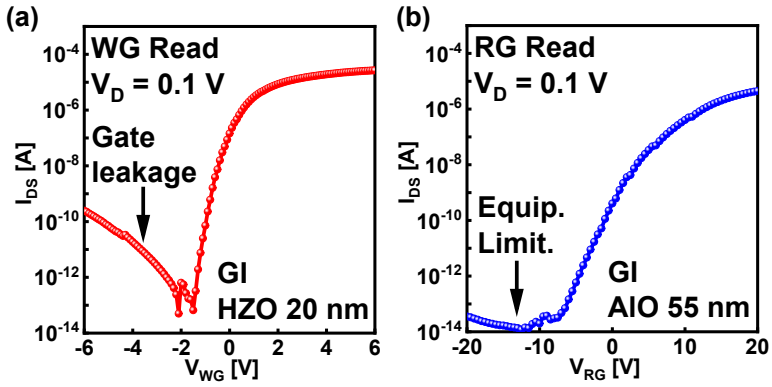

Figure S2. I_D-V_G curves of dual-port FeNAND devices with **(a)** WG and **(b)** RG read.

Figure S2a-S2b show I_D-V_G curves of dual-port FeNAND devices with WG and RG read. When WG is used as a read gate, the I_D-V_G curves with WG read has low subthreshold swings compared to the RG read due to the high gate dielectric capacitance of 20 nm thick HZO. However, relatively thin HZO causes gate leakage components, indicating high off-current level. On the other hand, I_D-V_G curves with RG read show low off-current level below 10^{-13} A, which is a measurement limitation of equipment, due to the thick AlO gate dielectric.

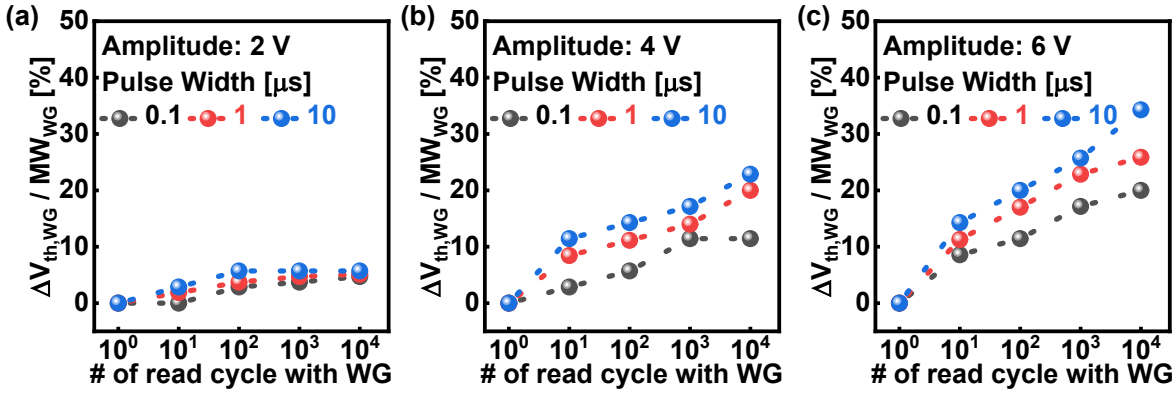

Figure S3. Disturbance behaviors of single-port FeNAND devices as a function of pulse width with various pulse amplitudes of **(a)** 2 V, **(b)** 4 V, and **(c)** 6 V.

Figure S3a-S3c show disturbance behaviors of single-port FeNAND devices as a function of pulse width and amplitude. When a low voltage of 2 V was applied, a minimal disturbance of less than 10% was observed. In contrast, when higher voltages of 4V and 6V were applied, the disturbance increased significantly, reaching up to 34.3%. This indicates that single-port FeNAND devices are susceptible to disturbance problems.

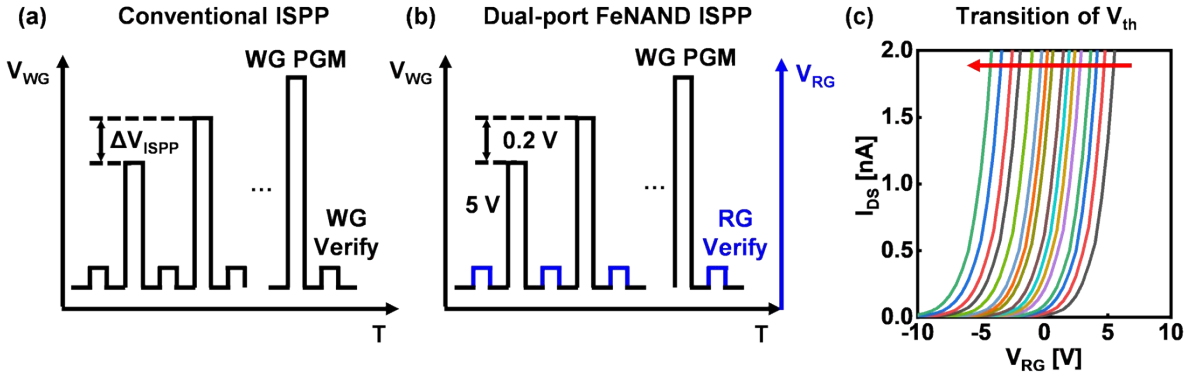

Figure S4. ISPP schematics of **(a)** conventional NAND devices and **(b)** dual-port FeNAND devices. **(c)** Transition of threshold voltages of dual-port FeNAND devices during the QLC operations.

Figure S4a and **S4b** show ISPP schematics of conventional NAND devices and dual-port FeNAND devices. In general, the ISPP is used to achieve tight V_{th} distribution in multiple-level operations, such as MLC and beyond. Furthermore, in our dual-port FeNAND devices, the RG is used as a verifying gate to amplify the MW and inhibit the read disturbance. In the characterization of QLC operations, we applied a bias by increasing the pulse amplitude from 5 V in 0.2 V steps and the pulse width was set to 1 μs. The transition of V_{th} measured with the ISPP method is shown in **Figure S4c**. Due to the ISPP method, the uniform V_{th} shift was measured.

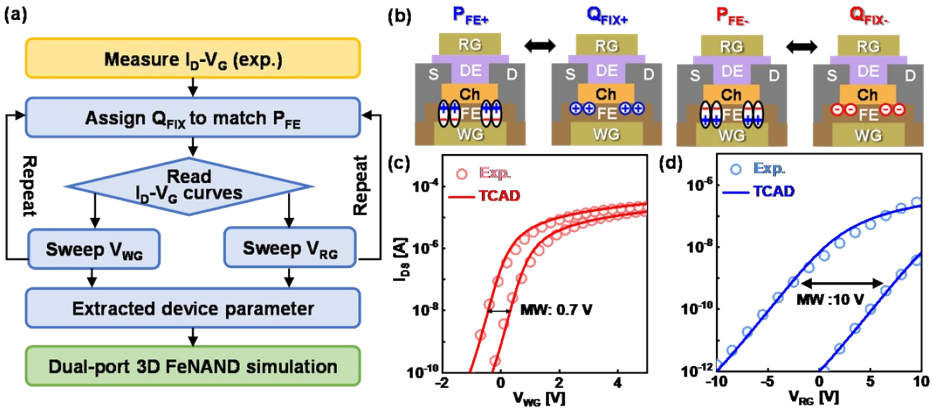

Figure S5. (a) Simulation framework of dual-port 3D FeNAND. **(b)** Methodology of a fixed charge for polarization switching simulation. Verification of consistency between TCAD models and experimental data with **(c)** WG and **(d)** RG read operation. TCAD parameters extracted from experimental data were used to simulate a dual-port 3D FeNAND array.

Figure S5a and **S5b** show the 3D FeNAND simulation framework and remnant polarization (P_{FE}) implementing technique with fixed charge (Q_{FIX}), respectively. Firstly, we performed the calibration between experimental data and TCAD simulation. For implementing the MW caused by P_{FE} in experimental data, the P_{FE} was matched with Q_{FIX}. The calibration results between TCAD and experimental data with WG and RG are shown in **Figure S5c** and **S5d**.

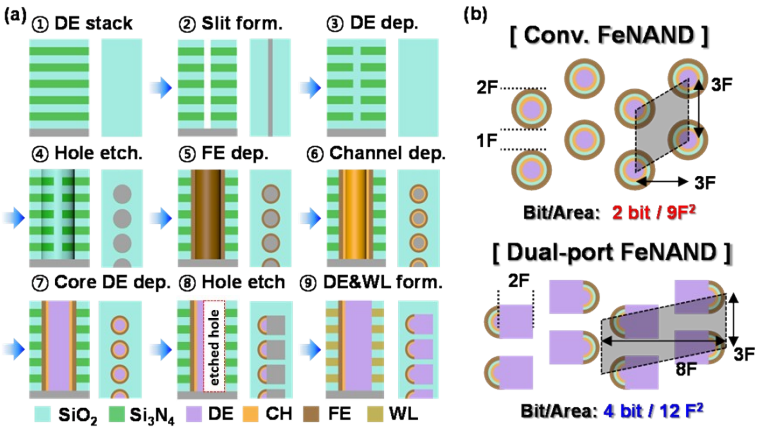

Figure S6. (a) Cross-sectional and top views of dual-port 3D FeNAND integration process. **(b)** Comparison of the number of bits per unit cell area between conventional FeNAND and dual-port FeNAND. Although the unit cell size of dual-port FeNAND is large, the number of bits per area can be further increased due to the QLC and beyond.

Figure S6a shows cross-sectional & top views of the dual-port 3D FeNAND integration process. Most of the process is the same as the conventional process. In the 2nd step, a slit is formed to divide WG and RG from the word line. In the 8th step, the second hole is etched and filled with dielectric which will be RG gate insulator. Finally, Si_3N_4 layers are etched away and replaced with the WL metal at the 9th step. The proposed dual-port FeNAND occupies a relatively large unit cell area compared to conventional FeNAND. However, since the dual-port FeNAND is capable of QLC operation, the number of bits per unit cell area was considered for a fair comparison as depicted in **Figure S6b**. As a result, we found that dual-port FeNAND has 4 bits per unit cell area as compared to typical FeNAND (2 bits/$9F^2$), which is the improvement of 50%.

Reference

1. Joh, H.,Nam, S.,Jung, M.,Shin, H.,Cho, S. H.,Jeon, S., Ferroelectric Hafnia-Based M3D FeTFTs Annealed at Extremely Low Temperatures and TCAM Cells for Computing-in-Memory Applications. *ACS Applied Materials Interfaces* **2023,** *15* (44), 51339-51349.