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Supporting information

Well-balanced Hole and Electron Charge Transport in an Organic P-type-Insulator-N-type Layered Sandwich Structure

Jaechan song [a] , Youngmin Han [a], and Hocheon Yoo [a, *]

[a] Department of Electronic Engineering, Gachon University, Seongnam 13120, Republic of Korea

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* Corresponding author

Email address: hyoo@gachon.ac.kr (H. Yoo)

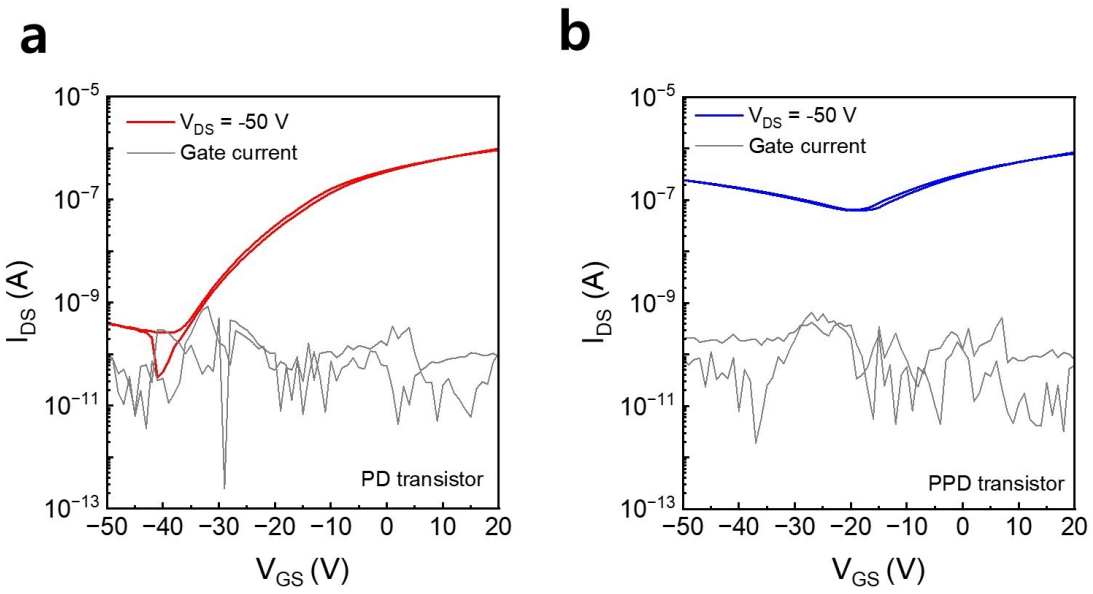


Fig. S1 (a) Transfer curve of PD transistor with gate leakage current in p-type mode operation, gate-source voltage (V_{GS}) ranging from -50 V to 20 V, drain-source voltage (V_{DS}) at -50 V. (b) Transfer curve of PPD transistor with gate leakage current in p-type mode operation, V_{GS} ranging from -50 V to 20 V, V_{DS} at -50 V.

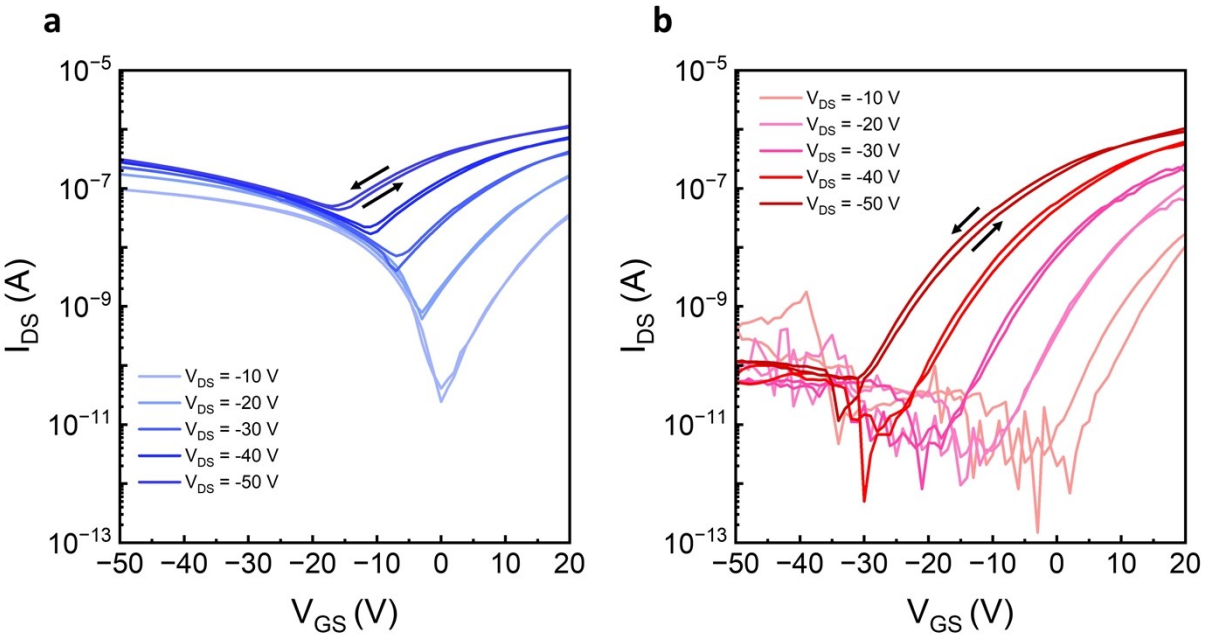


Fig. S2 Dual sweep transfer curve of (a) PD and (b) PPD transistor with gate leakage current in p-type mode operation, V_{GS} ranging from -50 V to 20 V, V_{DS} increasing from -10 V to -50 V

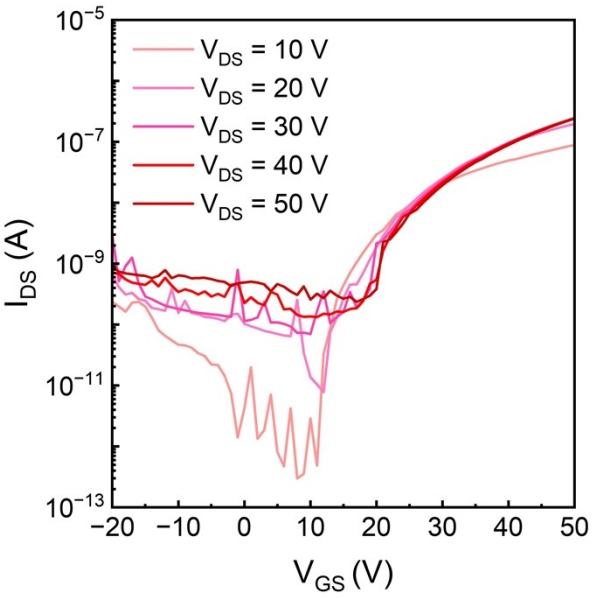


Fig. S3 Transfer curve of a PD transistor in n-type mode with V_{GS} increasing from -20 V to 50 V and V_{DS} increasing variations.

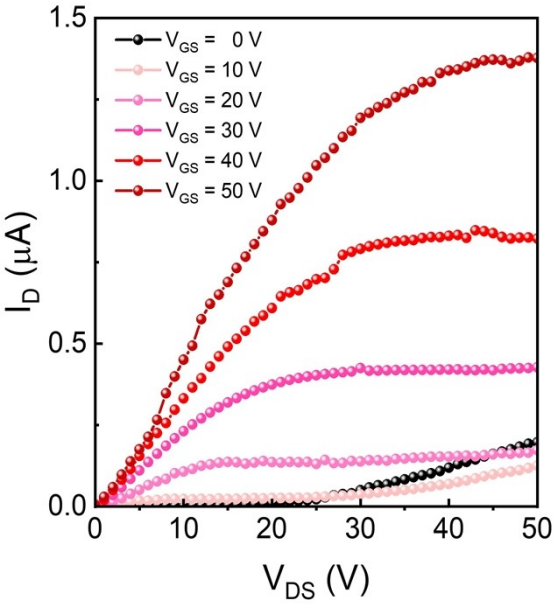


Fig. S4 Output curve of a PD transistor in n-type mode with V_{DS} from 0 V to 50 V and V_{GS} variations.

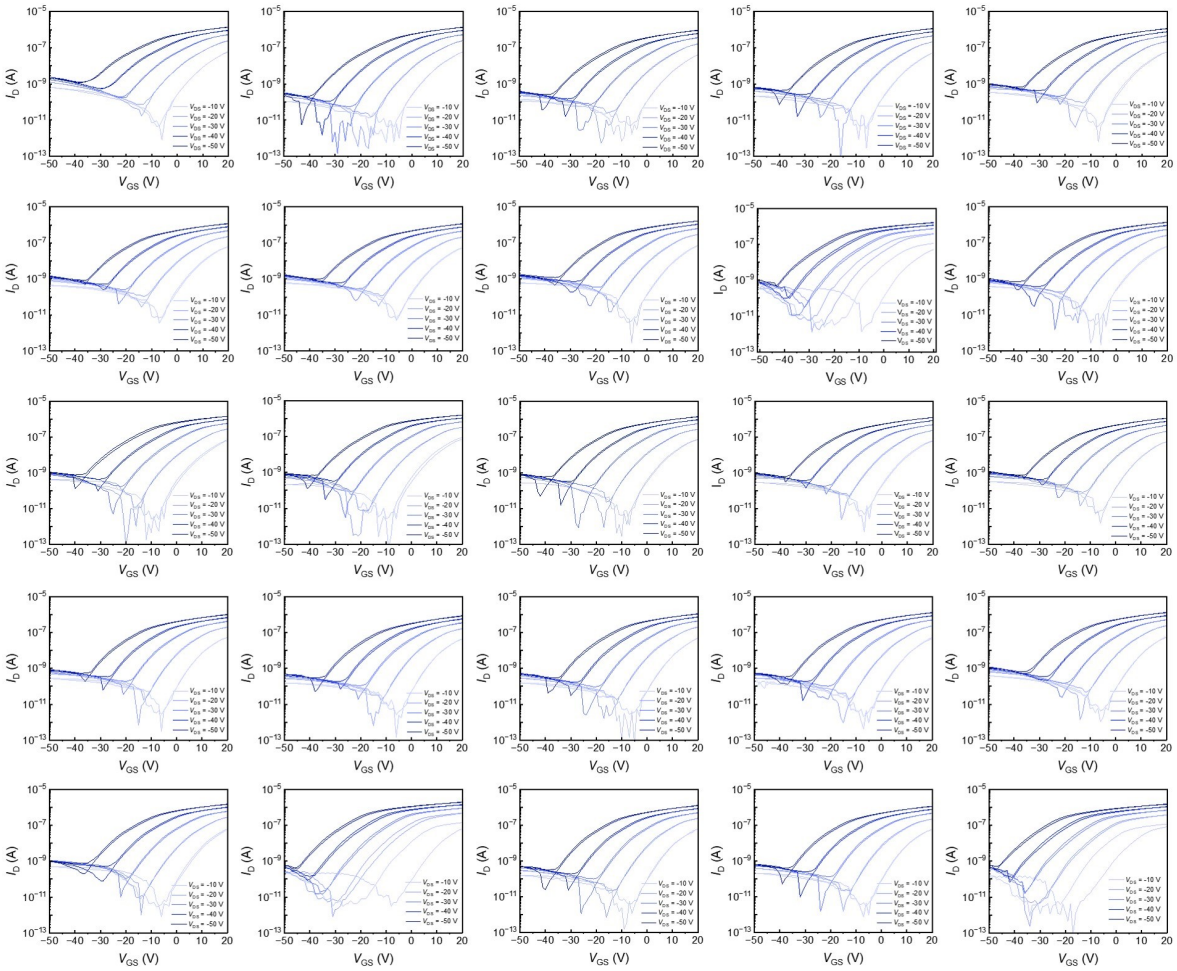
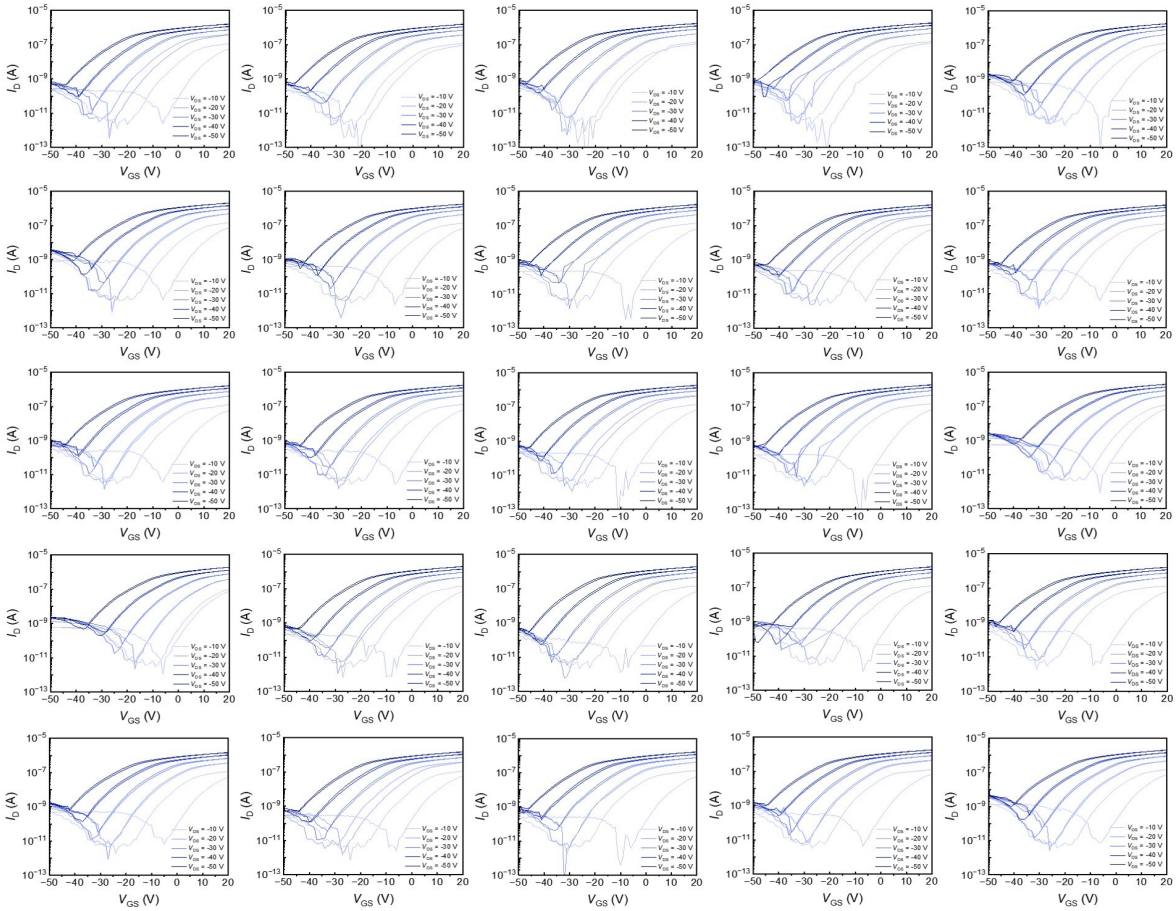


Fig. S5 50 transfer curves measured to evaluate the uniformity of PD transistors and extract reliable electrical parameters


I_D (A)
V_{GS} (V)
V_{DS} = -10 V
V_{DS} = -20 V
V_{DS} = -30 V
V_{DS} = -40 V
V_{DS} = -50 V

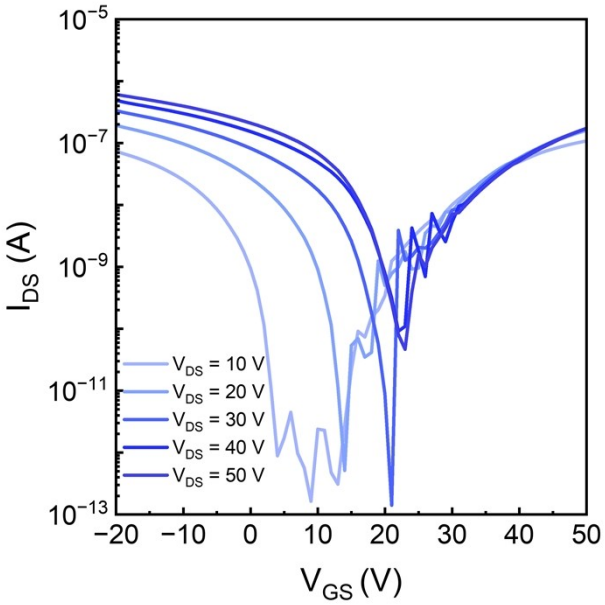


Fig. S6 Transfer curve of a PPD transistor in n-type mode with V_{GS} increasing from -20 V to 50 V and V_{DS} increasing variations.

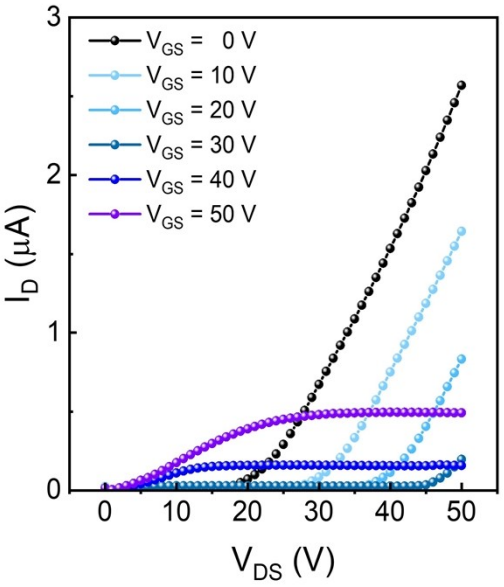


Fig. S7 Output curve of a PD transistor in n-type mode with V_{DS} from 0 V to 50 V and V_{GS} variations.

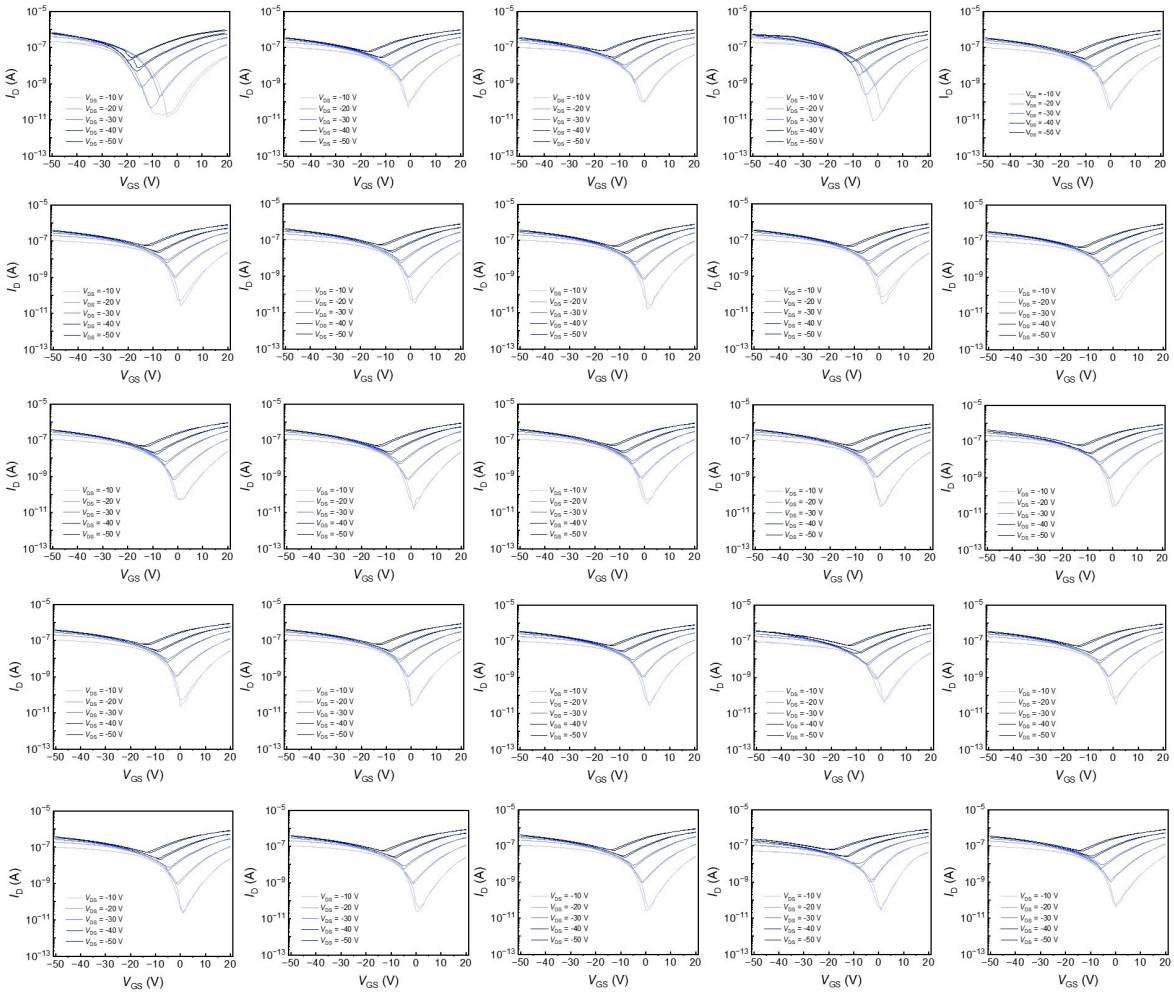
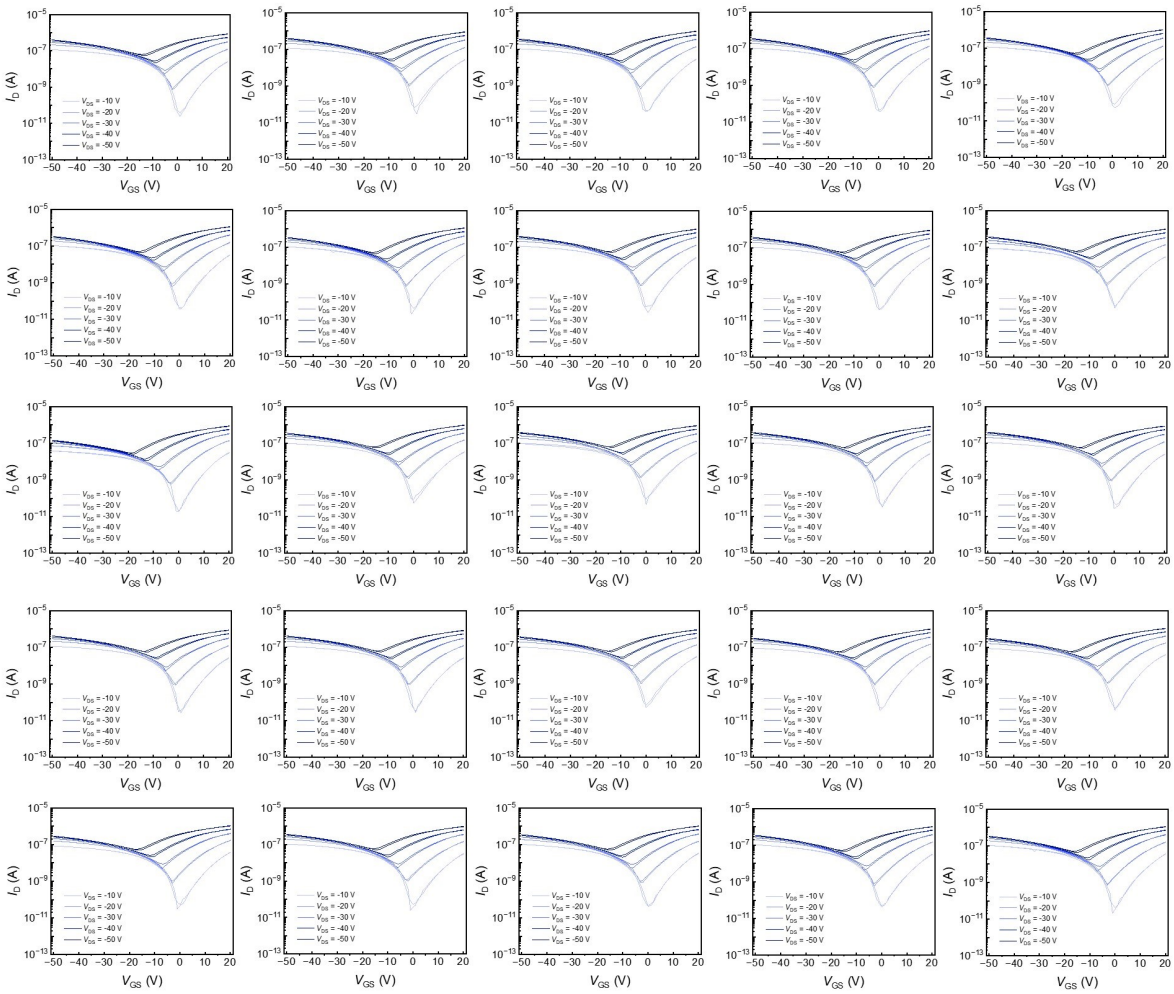


Fig. S8 50 transfer curves measured to evaluate the uniformity of PPD transistors with balanced hole and electron currents due to the parylene interlayer and to extract reliable electrical parameters.


I_D (A)
V_{GS} (V)
V_{DS} = -10 V
V_{DS} = -20 V
V_{DS} = -30 V
V_{DS} = -40 V
V_{DS} = -50 V

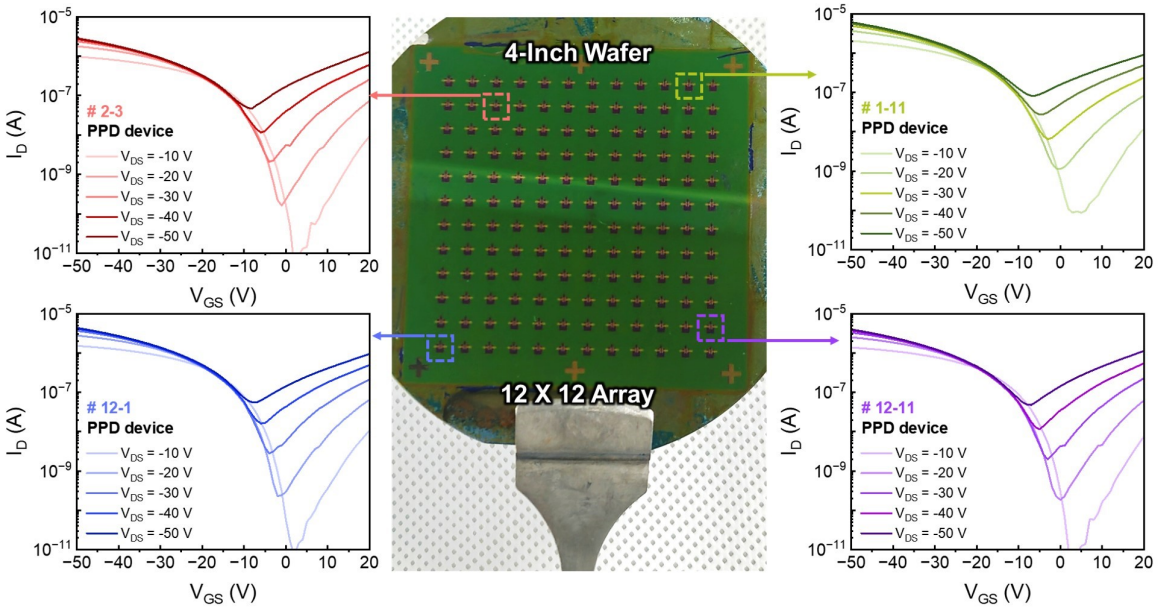


Fig. S9 The transfer curves of four PPD transistors located at the four edges of a 4-inch wafer, the voltage bias conditions of V_{GS} from -50 V to 20 V and V_{DS} from -10 V to -50 V.

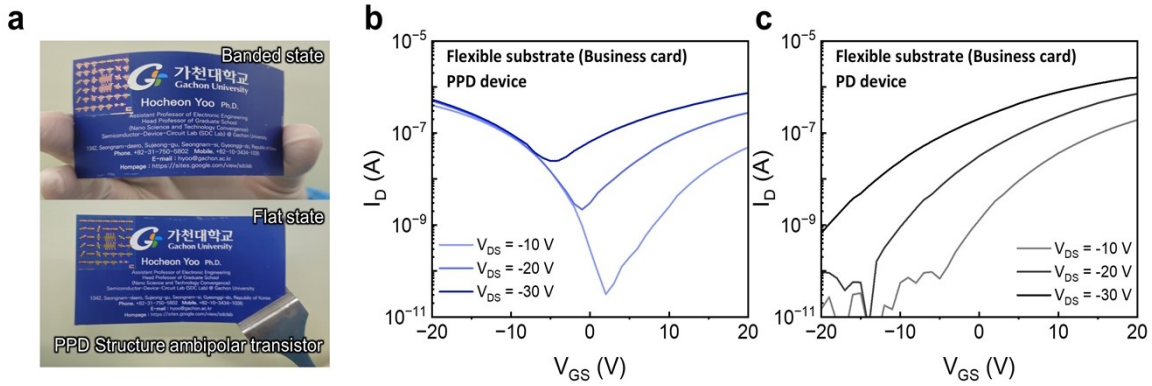


Fig. S10 (a) actual images of PPD transistor with banded state, flat state. Transfer curve of (b) PPD and (c) PD transistor realized on the flexible substrate (Business card) with V_{GS} from -20 V to 20 V, V_{DS} from -10 V to -30 V.

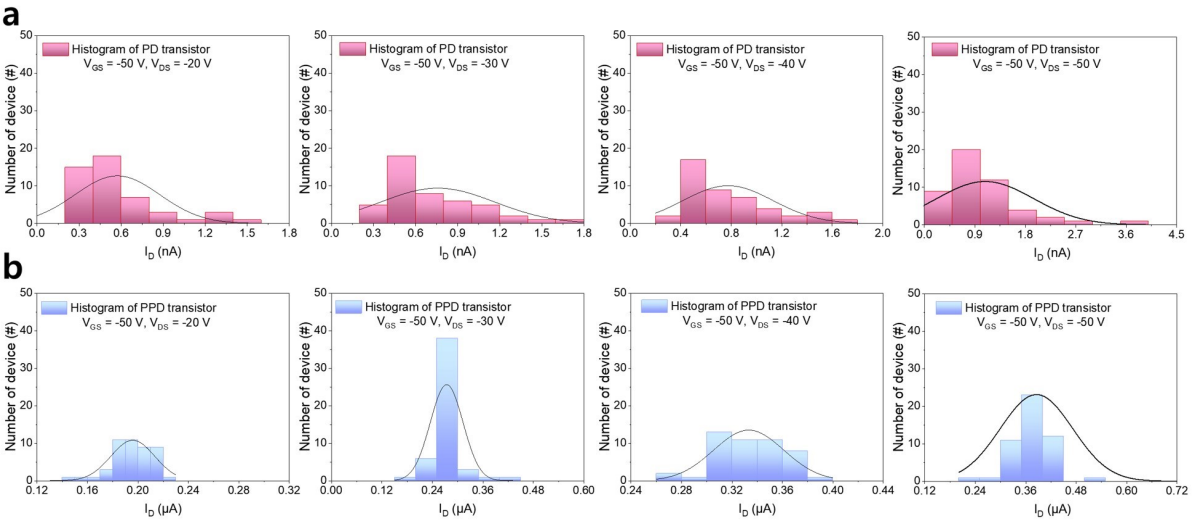


Fig. S11 Histogram of drain current extracted from the (a) PD and (b) PPD transistor, the voltage bias condition was V_{GS} at -50 V, V_{DS} increasing from -20 V to -50 V.

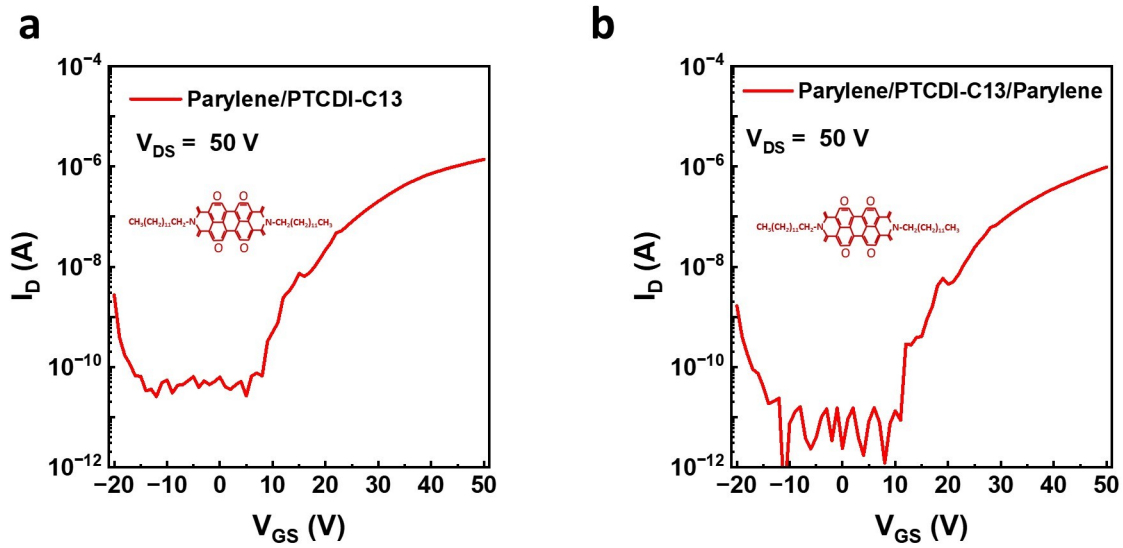


Fig. S12 (a) Transfer curve of parylene/PTCDI-C13 transistor at V_{DS} = 50 V (b) Transfer curve of parylene/PTCDI-C13/parylene transistor at V_{DS} = 50 V.

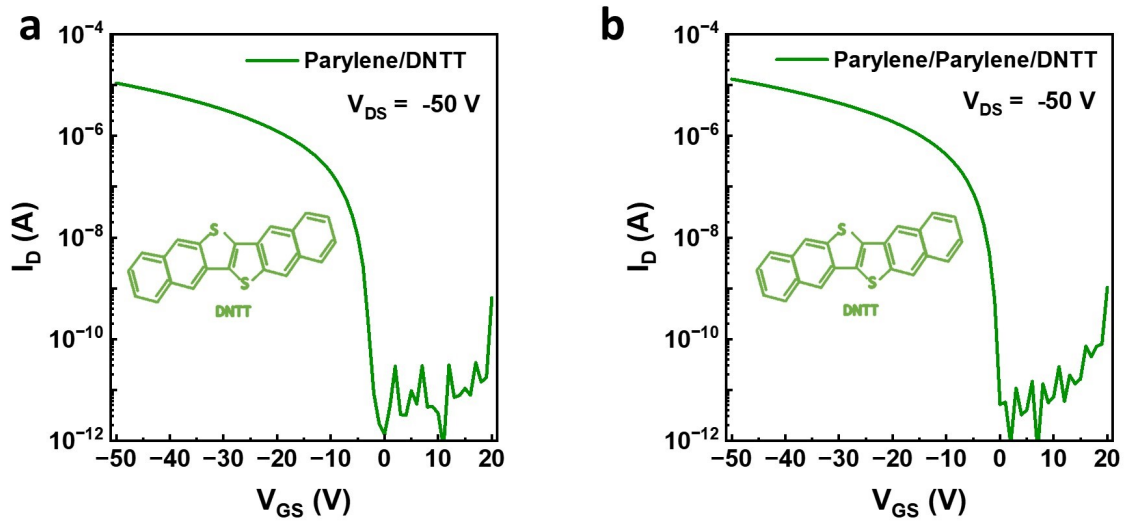


Fig. S13 (a) Transfer curve of parylene/DNTT transistor at V_{DS} = -50 V (b) Transfer curve of parylene/parylene/DNTT transistor at V_{DS} = -50 V.

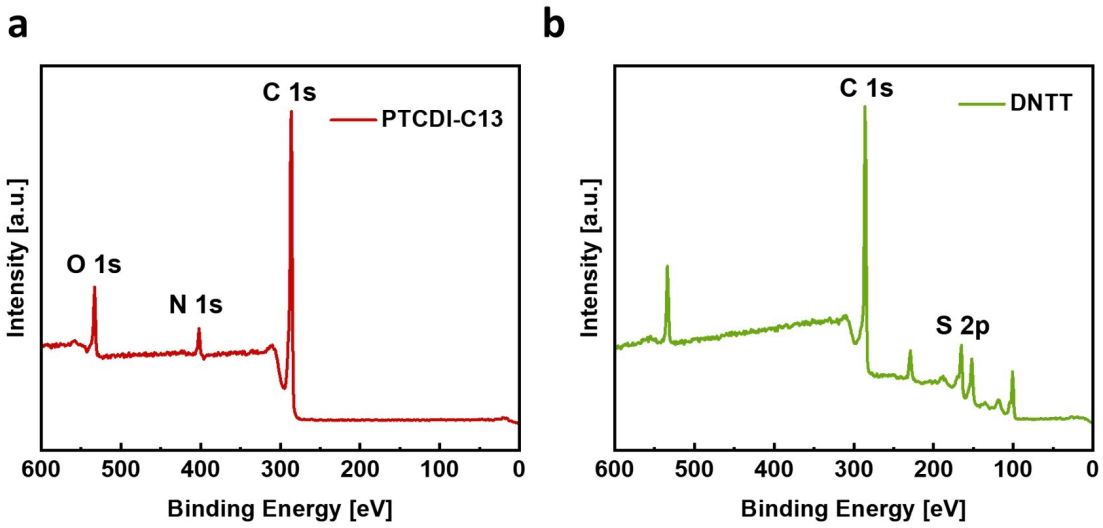


Fig. S14 XPS results for compositional analysis of organic small molecules (a) PTCDI-C13 and (b) DNTT

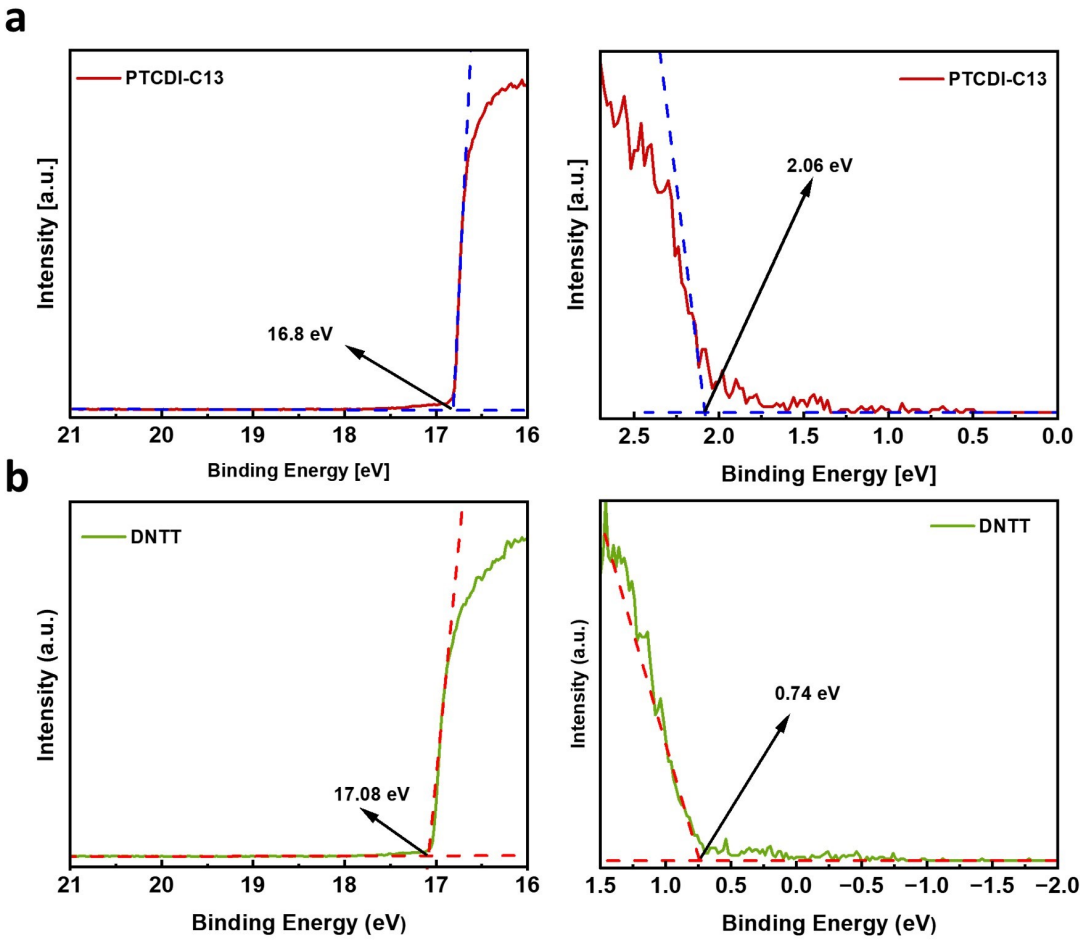


Fig. S15 Analysis of (a) PTCDI-C13 and (b) DNTT UPS examined to extract energy band diagrams.

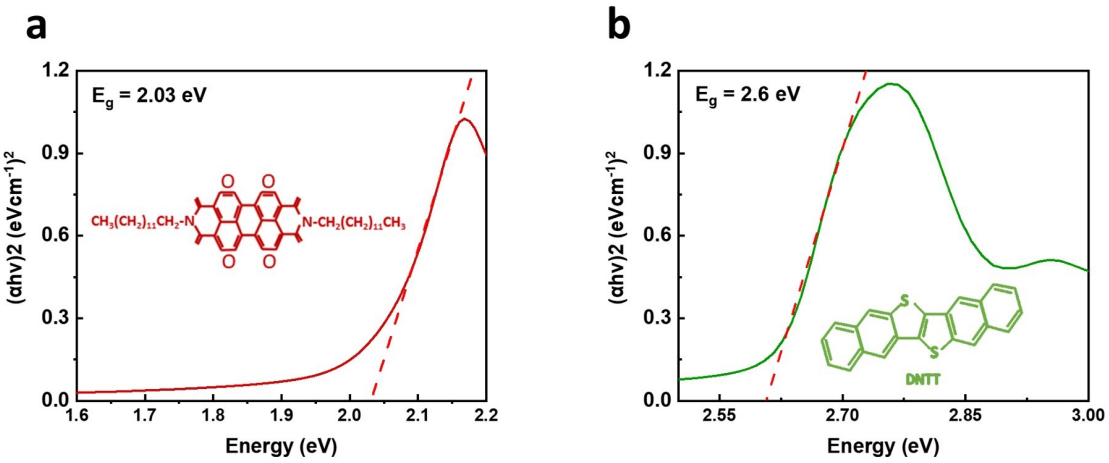


Fig. S16 UV-visible results of (a) PTCDI-C13 and (b) DNTT analyzed to investigate the energy bandgap.

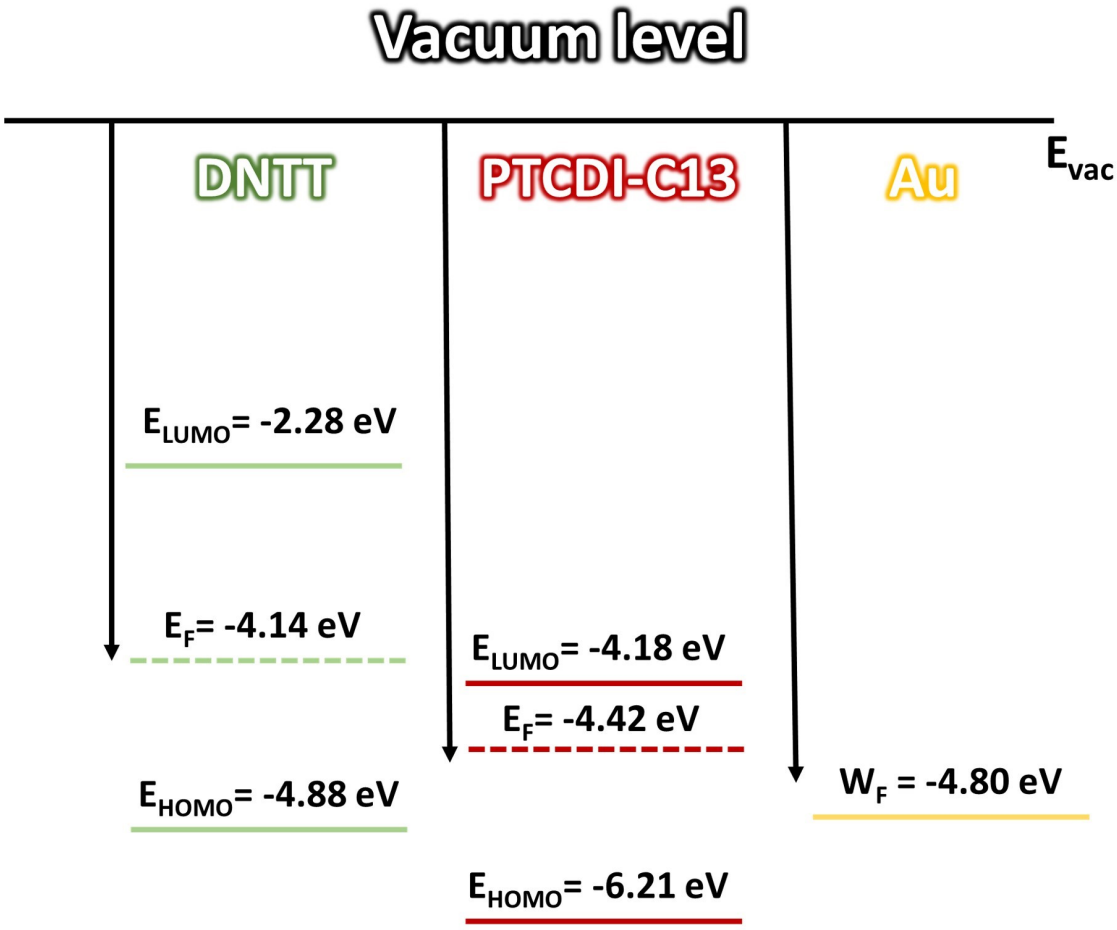


Fig. S17 Energy band diagram of DNTT, PTCDI-C13, Au.

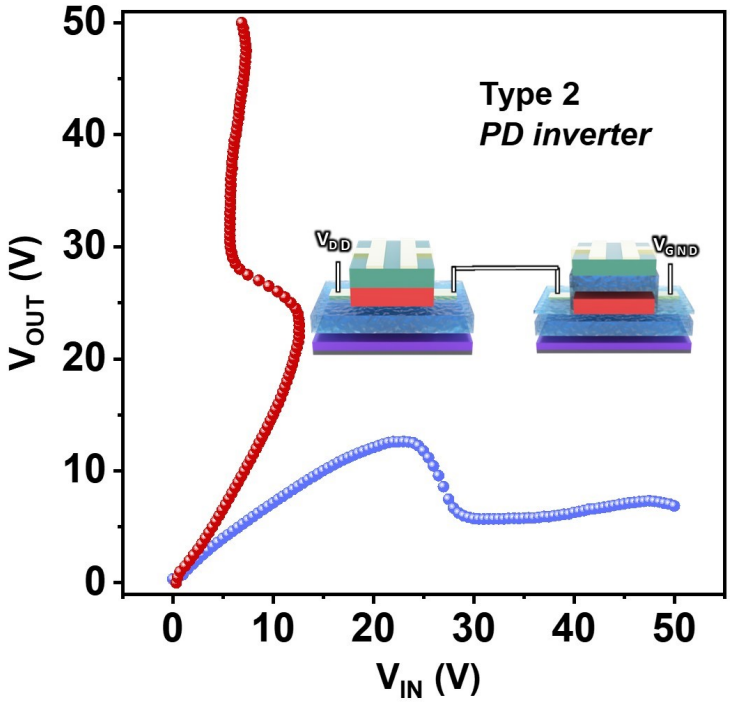


Fig. S18 Voltage transfer curve of a Type 2 inverter with PD transistor as pull-up device and PPD transistor as pull-down device.

Semiconductor	V_{DS}(V)	$I_{hole}/I_{electron}$ ($A \cdot A^{-1}$)	V_{TS} (V)	Reference
PDPP-Pya (ambipolar)	-60	≈ 10	-22.2	[1]
4HNi (ambipolar)	-60	≈ 10	-10	[2]
PDITTTT (n-type) / C8-BTBT (p-type)	-180	N/A	-25	[3]
ZnO (n-type) / PDPPBTT (p-type)	-30	≈ 10	-10	[4]
C6-DPA (p-type) / F16CuPc (n-type)	-60	≈ 10	-5	[5]
MoS_2 (n-type) / BTBT (p-type)	-3	N/A	-6	[6]
DNTT (p-type)/ PTCDI-C13(n-type)	-10	0.004	-11	***This work***
DNTT (p-type) /parylene (dielectric)/ PTCDI-C13(n-type)	-10	1.08	0	***This work***

Table S1 Table for the recent fabrication methods and performance trends of ambipolar transistors.

PD transistor	I_{Hole} (V_{GS} = -50 V)	$I_{Electron}$ (V_{GS} = 20 V)	V_{TS}
V_{DS} = -20 V	6.61 $\pm$ 2.16 $\times$ 10^{-10} A	3.45 $\pm$ 1.04 $\times$ 10^{-7} A	-23 $\pm$ 2.83 V
V_{DS} = -30 V	8.65 $\pm$ 6.67 $\times$ 10^{-10} A	6.73 $\pm$ 1.74 $\times$ 10^{-7} A	-29 $\pm$ 6.04 V
V_{DS} = -40 V	9.90 $\pm$ 7.83 $\times$ 10^{-10} A	1.09 $\pm$ 0.25 $\times$ 10^{-6} A	-35 $\pm$ 5.20 V
V_{DS} = -50 V	1.08 $\pm$ 0.87 $\times$ 10^{-9} A	1.57 $\pm$ 0.32 $\times$ 10^{-6} A	-42 $\pm$ 4.56 V

Table S2 Specifying the average values of I_{Hole} when V_{GS} is -50 V and V_{DS} is increased from -20 V to -50 V, $I_{Electron}$ when V_{GS} is 20 V and V_{DS} is increased from -20 V to -50 V, and V_{TS} when V_{DS} is increased from -20 V to -50 V in 50 PD transistor.

PPD transistor	I_{Hole} (V_{GS} = -50 V)	$I_{Electron}$ (V_{GS} = 20 V)	V_{TS}
V_{DS} = -20 V	$2.00 \pm 0.34 \times 10^{-7}$ A	$1.37 \pm 0.84 \times 10^{-8}$ A	-2.18 ± 2.83 V
V_{DS} = -30 V	$2.74 \pm 0.39 \times 10^{-7}$ A	$3.45 \pm 0.46 \times 10^{-7}$ A	-5.98 ± 2.62 V
V_{DS} = -40 V	$3.39 \pm 0.56 \times 10^{-7}$ A	$6.04 \pm 0.71 \times 10^{-7}$ A	-9.54 ± 2.56 V
V_{DS} = -50 V	$3.86 \pm 0.86 \times 10^{-7}$ A	$9.45 \pm 1.07 \times 10^{-7}$ A	-14 ± 2.45 V

Table S3 Specifying the average values of I_{Hole} when V_{GS} is -50 V and V_{DS} is increased from -20 V to -50 V, $I_{Electron}$ when V_{GS} is 20 V and V_{DS} is increased from -20 V to -50 V, and V_{TS} when V_{DS} is increased from -20 V to -50 V in 50 PPD transistor.

- Reference

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