Electronic Supplementary Information

Deoxyribonucleic acid brick crystal-based memristor as an artificial synapse for neuromorphic computing

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DNA strand sequences

CCAGGTTAAGTGGCTCAATCATACTCACGGTT	1, 23
AACTGTTGTGTCCTATGTTTACTTAGGGATGG	1, 39
TACGAACTCAACGCACGCTCGGGTAGTCTCAA	3, 23
GAAGATAGAGAGCATAAATTCGCTAAACCGGA	3, 39
AAAGTATCCGCATCTCACTCAGTGATCGAGTA	5, 23
TTCATGTCGCCTTTTCGAACGGTGACACACTT	5, 39
GTGTTCATTCAGAGTAGCGGAAATATGGCCGC	7, 23
TTCGGTGCGCAGCGGGCCGCCTGTAACGCTTA	7, 39
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ACAGGCGGTACTCGATGGGCTGATCCCGCAAC	6, 31
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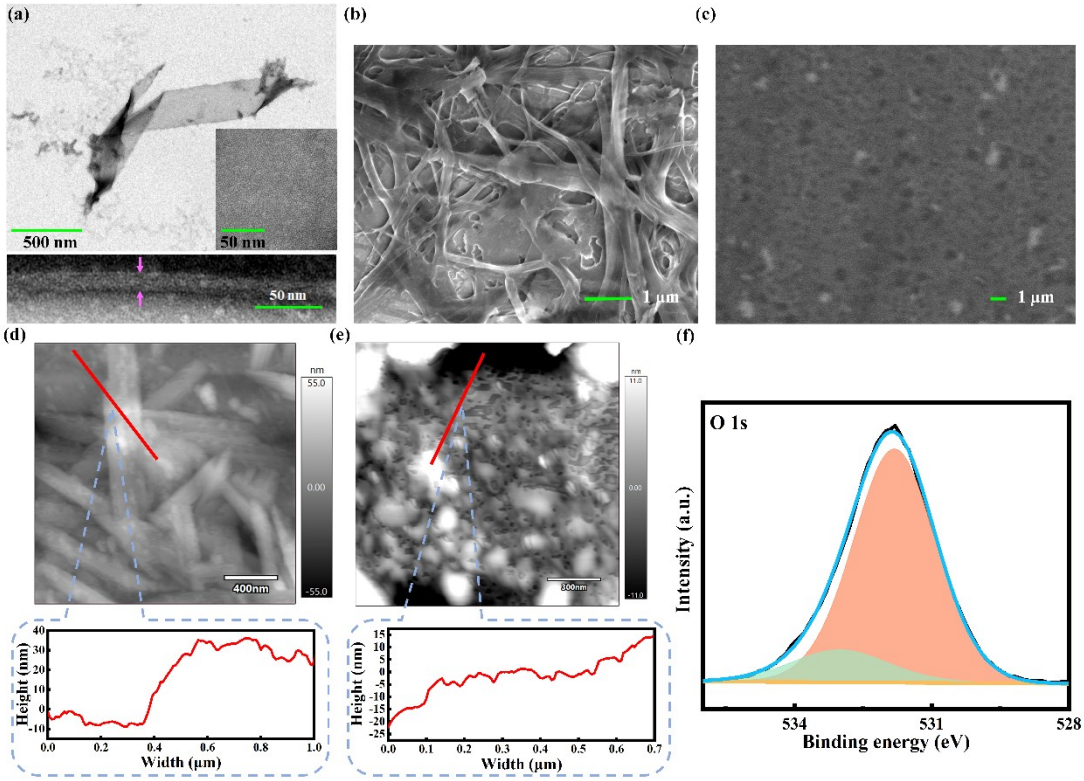

Fig. S1 (a) TEM images of the synthesized DNAbc, the pink arrows indicate positions for thickness measurements of the crystals. (b) SEM image of the DNAbc functional layer films. (c) SEM image of the dsDNA functional layer films. (d) and (e) are AFM images of the DNAbc and dsDNA functional layer films, the thickness are measured by AFM Height sensor. (f) O 1s core-level spectra of the DNAbc films.

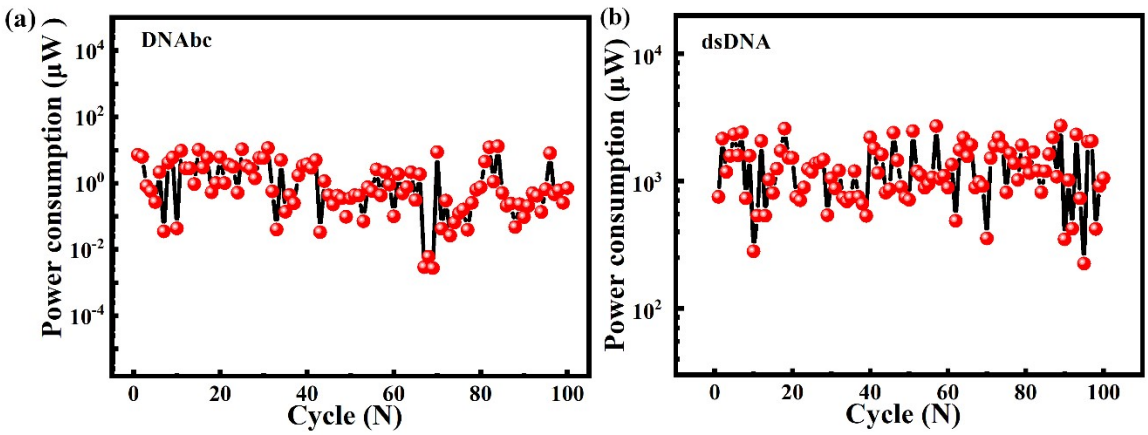

Fig. S2 (a) and (b) are statistical analysis of the set power consumption of DNAbc- and dsDNA-based device, respectively.

Table S1 Key parameters compared with other memristors based on organic and inorganic materials.

Device Structure	Switching ratio	Set current	P_{Set}	Year/Ref.
Al/Polymer membrane/ITO	10^3	10 μA	10 μW	2020[1]
Al/TiO_2-few layer Graphene-DNA/Pt	34.8	1 mA	3 mW	2021[2]
Au/$(IFA)_3PbI_5$/ITO	10^3	1 mA	0.2 mW	2021[3]
Ag/Silk fibroin/ITO	20	3 mA	4.2 mW	2021[4]
Ag/$AgNO_3$ doped iota-carrageenan/ITO	<10	12 μA	3.6 μW	2022[5]
Au/Polyimide/Au	10^2	5 mA	3 mW	2022[6]
Al/Honey (90 °C)/ITO	10^4	10 μA	30 μW	2022[7]
ITO/Polyacrylic acid/Polyethylenimine/ITO	10^2	1 mA	1 mW	2022[8]
Ag/$[(TZ\text{-}H)_2(PbBr_4)]_n$(TZ = 1H-1,2,4-triazole)/FTO	3.19×10^2	37 mA	35.52 mW	2022[9]
Ag/DNA-cetyltrimethylammonium chloride/ITO	N	N	N	2023[10]
Ag/Poly(9-vinylcarbazole): tetracyanoquinodimethane/ITO	10^3	37.6 μA	20.7 μW	2023[11]
ITO/Poly(acrylic acid)-Ca^{2+}/ITO/glass	10^2	0.1 mA	50 μW	2023[12]
Al/DN@poly(diallyldimethylammonium)bis(trifluoromethanesulfonyl)imide/ITO	10^3	3.16 μA	4.74 μW	2024[13]
Ag/MoO_3/Graphene	10^4	0.1 mA	50 μW	2024[14]
EGaIn/$MAPbI_3$/Poly(3,4-ethylenedioxythiophene): poly(4-styrenesulphonate)/ITO	10^4	10 μA	5.6 μW	2024[15]
Ag/Py-Covalent organic polymer/ITO	10^2	7 μA	5.81 μW	2024[16]
Ag/DNAbc/Graphene	10^4	0.96 μA (average set current of 100 cycles)	2.17 μW (average P_{Set} of 100 cycles)	This work

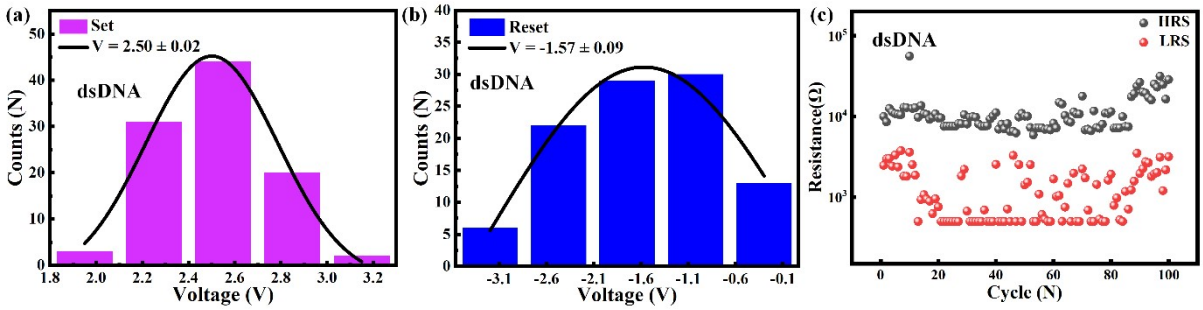

Fig. S3 (a) and (b) are gaussian distribution histogram of V_{Set} and V_{Reset} for dsDNA-based device. (c) Resistance statistical analysis of HRS and LRS for dsDNA-based device. The reading voltage is 0.5 V.

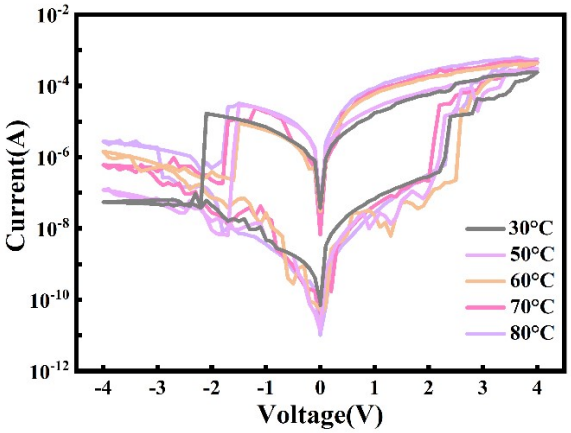

Fig. S4 The *I–V* curves of the device at 30 °C, 50 °C, 60 °C, 70 °C and 80 °C.

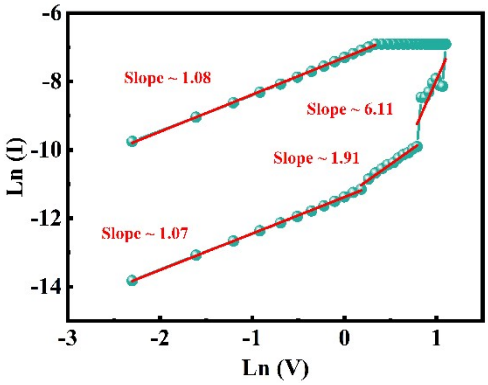

Fig. S5 The re-plotted HRS and LRS regions of the *I–V* curve of the dsDNA-based device using double-logarithmic scales and linear fitting of the curve.

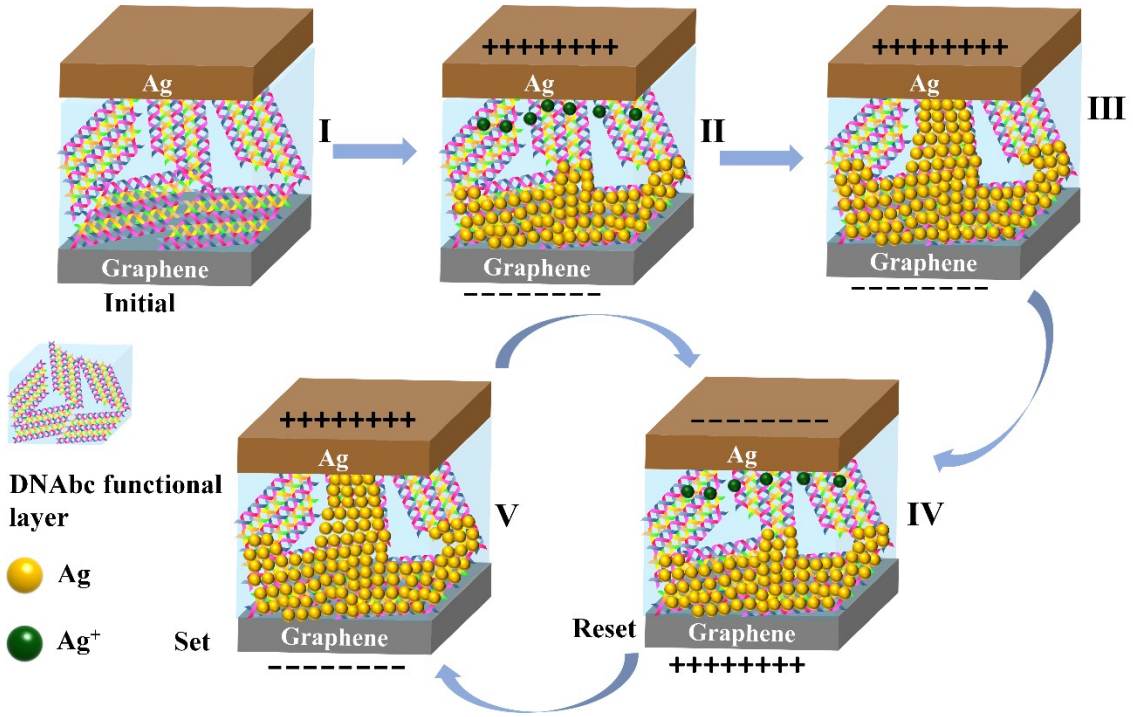

Fig. S6 The schematic diagram illustrating the RS mechanism of the DNAbc-based memristor.

Fig. S6 illustrate the resistance switching dynamic process of the DNAbc-based memristor. Fig. S6-I represents the initial state, and there is no Ag distribution in the functional layers of the DNAbc films. Upon application of a positive electric field, the oxidized Ag atoms (i.e., Ag^+) gradually migrate through the DNAbc layer to the vicinity of the graphene bottom electrode, and finally reduced to Ag atoms at the bottom electrode (Fig. S6-II). The orientation of DNA molecules in the DNAbc layer could provide efficient ionic pathways for Ag^+ transport when the applied voltage reached V_{Set}.[17] As the voltage increases, Ag atoms gradually accumulate and eventually extend to the Ag top electrode, which causes Ag CFs to form along DNAbc (Fig. S6-III). Upon the application of a negative voltage, the redox or Joule heat caused by Ag will lead to the fracture of the CFs, resulting in the switching of the device from LRS to HRS (i.e., Reset) (Fig. S6-IV). When a positive voltage is applied to the Ag top electrode again, Ag ions migrate downward and reduce to Ag at the graphene electrode, then the Ag atoms grow along the DNAbc layer to eventually short the Ag top electrode and produce Ag CFs, thereby converting the device from HRS to LRS (i.e., Set) (Fig. S6-V).

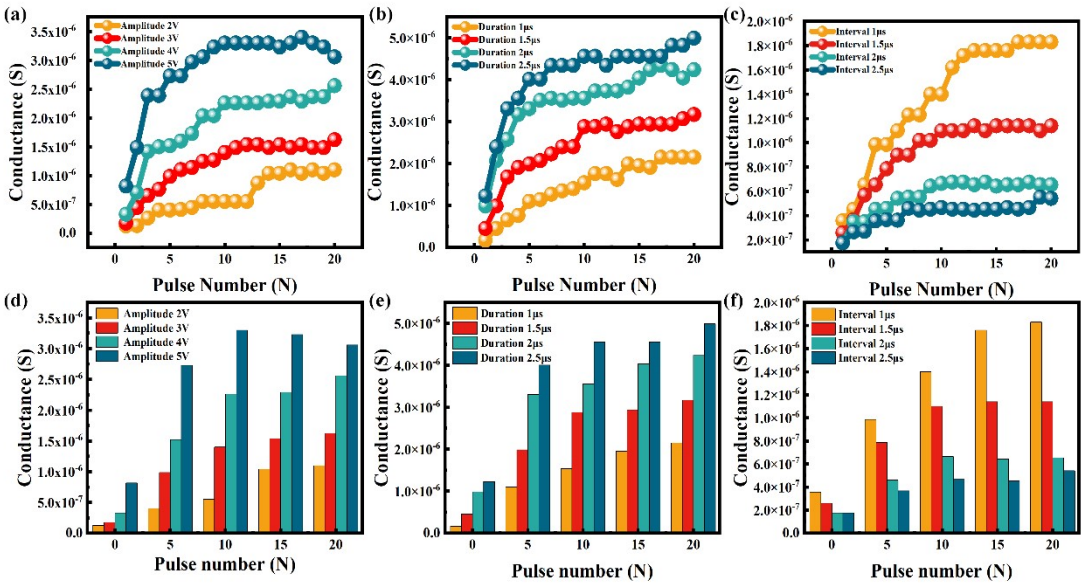

Fig. S7 The influence of pulse parameters on the modulation of conductance in the DNAbc-based memristor. (a), the relationship between conductance variation and pulse amplitudes, the pulse duration and interval are both 1 μs. (b), the relationship between conductance variation and pulse durations, the pulse amplitude is 3 V, the pulse interval is 1 μs. (c), the relationship between conductance variation and intervals, the pulse amplitude is 3 V, the pulse duration is 1 μs. (d)-(f), a train of pulses was used to measure the conductance of the device: (d) the pulse duration and interval are both 1 μs and different pulse amplitudes; (e) the pulse amplitude is 3 V, the pulse interval is 1 μs and different pulse durations; (f) the pulse amplitude is 3 V, the pulse duration is 1 μs and the different pulse intervals.

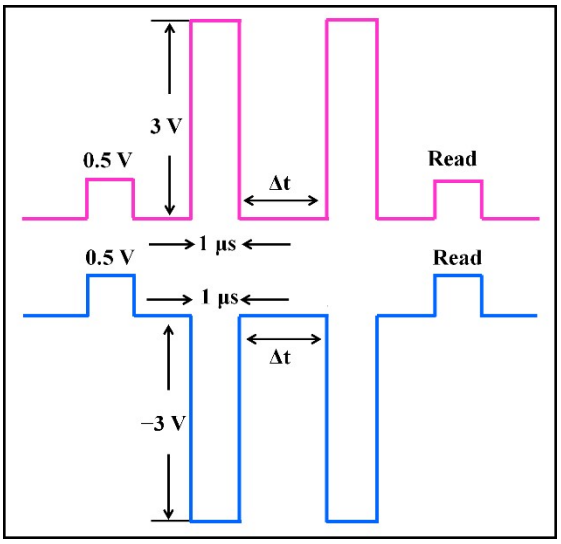

Fig. S8 Schematic diagram of the pulse waveforms for PPF and PPD measurements. The positive and negative waveforms are used for PPF and PPD measurements, respectively.

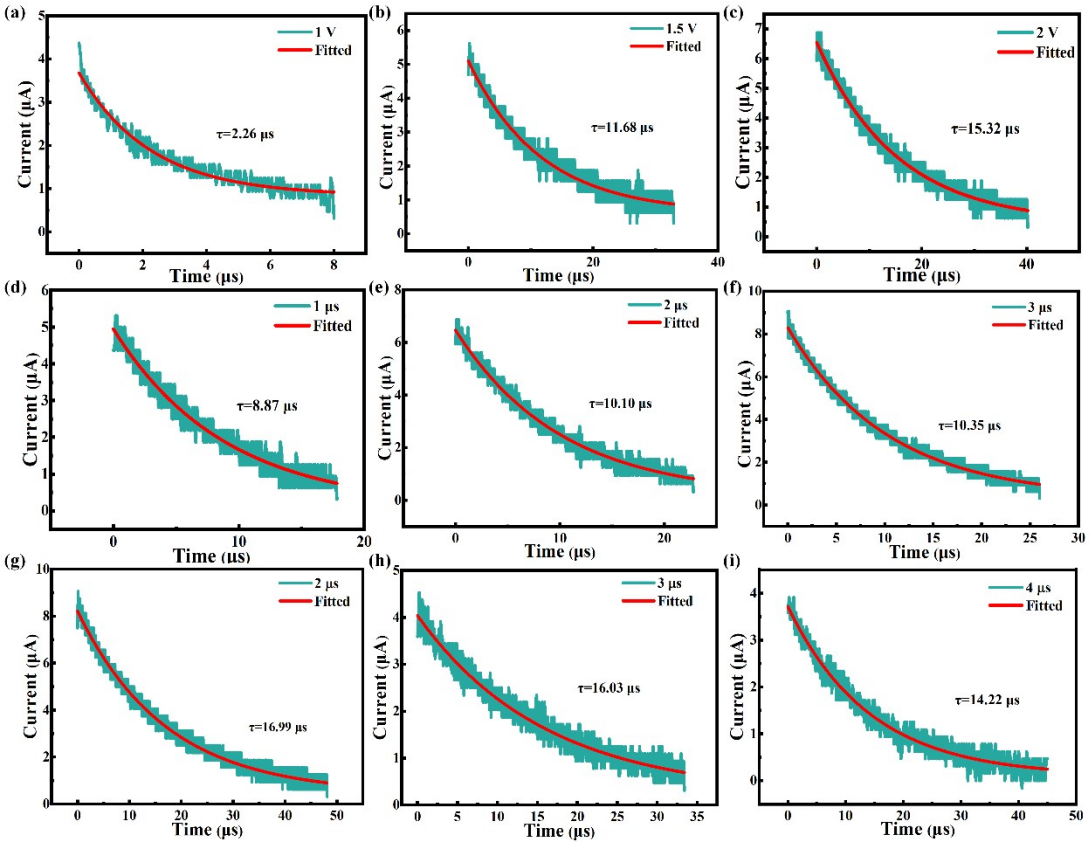

Fig. S9 The EPSC behavior of the device. (a)-(c), the relationship between the measurement retention tails (the cyan curves) and the fitting curves (the red lines) at different amplitudes (1, 1.5, and 2 V), the pulse durations and intervals are both 1 μs. (d)-(f), the relationship between the measurement retention tails (the cyan curves) and the fitting curves (the red lines) at different durations (1, 2, and 3 μs), the pulse amplitudes and intervals are fixed at 3 V and 4 μs, respectively. (g)-(i), the relationship between the measurement retention tails (the cyan curves) and the fitting curves (the red lines) at different intervals (2, 3, and 4 μs), the pulse amplitudes and durations are fixed at 3 V and 1 μs, respectively.

The reason that the same and different inputs result in different outputs[18]

Both the "AND" and "OR" logic gates exhibit comparable behavior when given the same input, where both inputs are either logic "1" or logic "0". For the same input, there is no voltage difference between them, resulting in the absence of any current in the circuit. Thus, the output voltage is equivalent to the input voltage. When both inputs are logic "0" ("1"), the input terminal receives the ground (power) voltage, the output voltage is ground (power), and the output logic state is logic "0" ("1"). When one input is logic "1" and the other is logic "0", the current flows from high voltage (terminal of the memristor with logic "1" input) to low voltage (terminal of the memristor with logic "0" input), thereby causing the resistance of the two memristors to change and resulting in different logic states.

Simulation process details

In this work, a single-layer artificial neural network was constructed, including an input layer (784 neurons), a hidden layer (300 neurons), and an output layer (10 neurons), and two datasets (MNIST and Digits) were used for evaluation. Each layer of the neural network is connected by artificial synapses, each with different synaptic weights at different locations. By learning and training on the dataset, we can consciously adjust the synaptic weights, enabling the network to reliably recognize numbers. The intersection of each horizontal and vertical bar in the crossbar is a memristor (as shown in Fig. 5(f)), and the synaptic weights are determined by Backpropagation, which is then mapped directly to the conductance value of the memristor. Based on Ohm's law and Kirchhoff's law, the crossbar containing the devices can directly implement vector-matrix multiplication, which is also an advantage over traditional architectures. The data used for the conductance parameter are the potentiation and depression behavior of the device (as shown in Fig. 3(b)), and the test was performed by applying twenty positive pulses then twenty negative pulses with the pulse amplitudes of ±2 V, duration and interval of 500 ns. We map and replace the conductivity parameter values of the device with the weight matrix obtained in the algorithm to implement the digital recognition process. The Learning rate used in the algorithm is 0.01, the clipping rate of conductivity parameters is 10%, and the mapping error is less than 5%.

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