Supplementary Information

Reducing MoS_2 FET contact resistance by stepped annealing to optimize device performance

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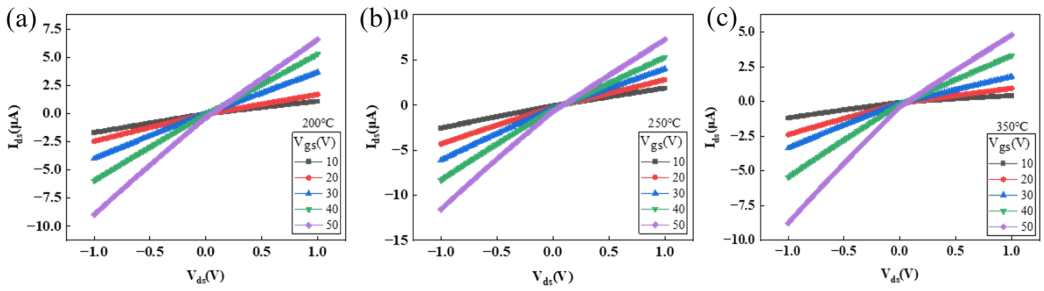

Fig S1. Output characteristics of the MoS_2 FET at varying V_{gs} after annealing at (a) 200°C (b) 250°C (c) 350°C.

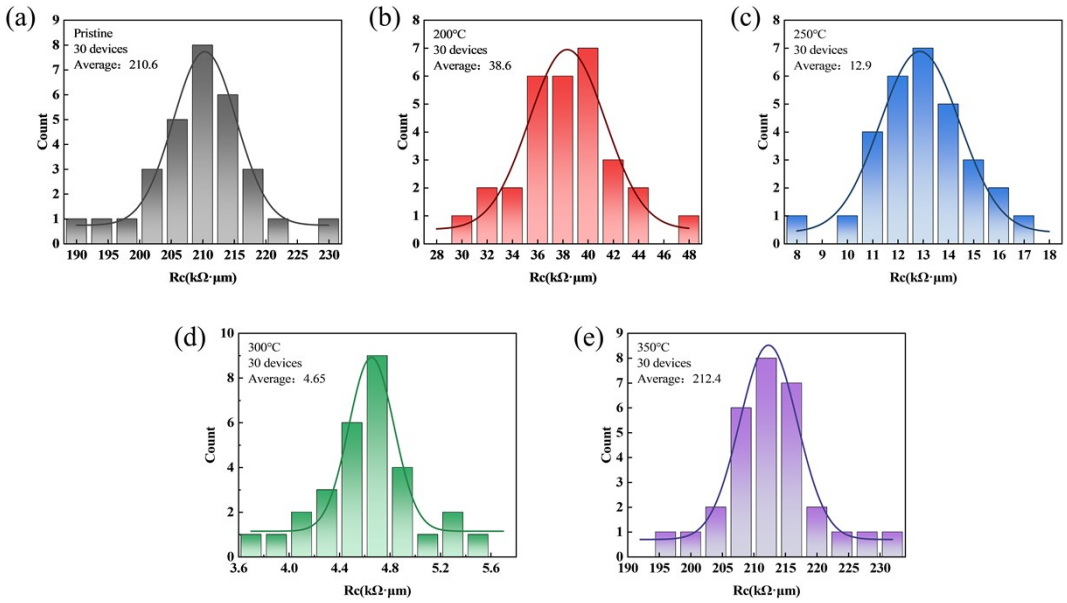

Fig S2. The statistical results of contact resistance of 30 devices (a) before annealing and after annealing at (b) 200°C, (c) 250°C, (d) 300°C, (e) 350°C.

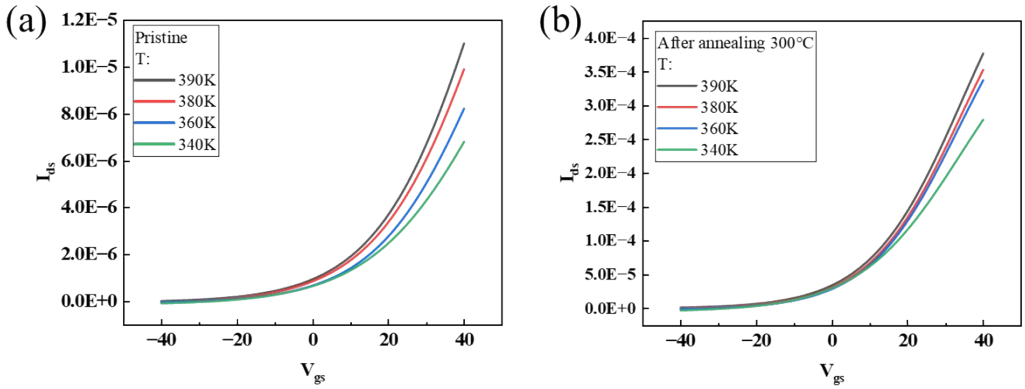

Fig S3. Transfer characteristic curves of MoS_2 FETs (a)before and (b)after 300℃ annealing at different operating temperatures.