Supplementary Information

Reservoir Computing Determined by Nonlinear Weight Dynamics in Gd-

doped CeO₂/CeO₂ Bi-layered Oxide Memristors

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Fig. S1. Cell-to-cell distribution the degree of potentiation results of the device using sputterdeposited bilayers and the device using sputter GDC/ALD CeO₂.



Fig. S2. Calculation of Schottky barrier height. *I*–*V* curves in the form of Schottky conduction with the relation of (**a**) $\log(J/A^*T^2)$ with respect to $E_{ox}^{0.5}$ at the temperatures of 297.15, 337.15, 357.15, 377.15 and 397.15 K with the band diagram of Pt/CeO₂ interface (inset) and (**b**) $\log(J/A^*T^2)$ with respect to 1/T. *I*–*V* curves in the form of Schottky conduction with the relation of (**c**) $\log(J/A^*T^2)$ with respect to $E_{ox}^{0.5}$ at the temperatures of 339.15, 359.15, and 379.15 K with the band diagram of Pt/GDC interface (inset) and (**d**) $\log(J/A^*T^2)$ with respect to 1/T.

For the Schottky conduction mechanism equation,

$$J = A^* T^2 exp\left[-\frac{q\phi_B}{k_b T} + \frac{1}{k_b T} \left(\frac{q^3 E_{ox}}{4\pi k_d \varepsilon_o}\right)^{1/2}\right]$$
(S1)

where *J* is the current density, A^* is effective Richardson constant, $q \phi_B$ is the Schottky barrier height, *T* is the absolute temperature, *q* is the elementary charge, ε_0 is the absolute dielectric permittivity of vacuum, E_{ox} is the electric field across the CeO₂ and GDC layer, k_b is the Boltzmann's constant, k_d is dynamic dielectric constant of CeO₂ and GDC layer as extracted from the slope of the graphs in Fig. S2a and Fig. S2c. To calculate Schottky barrier height $q\phi_B$, the curves were replotted in the relation $\log(J/A^*T^2)$ with respect to 1/T. From the slopes of these curves, the Schottky barrier heights of CeO₂ and GDC thin films were determined to be 0.3 eV and 0.55 eV.



Fig. S3. Experimental results of binary 4-bit input pulse data discrimination processing at four different pulse conditions. Experimental results of binary 4-bit input data discrimination processing by applying a binary 4-bit pulse train with a total of 16 states ([0000] to [1111]) for each the condition shown in the table. The read pulse amplitude and width are +2 V and 0.64 ms, respectively. The pulse condition of (**a**) +5 V×20 read at +2V, interval 10 s (condition 1), (**b**) +7 V×20 read at +2V, interval 10 s (condition 2), (**c**) +5 V×20 read at +2V, interval 5 s (condition 3), and (**d**) +5 V×10 read at +2V, interval 5 s (condition 4).





Fig. S4. In the case of pulse condition 1, response of GDC/CeO₂ memristors by repeatedly applying a pulse train to a binary 4-bit input for a total of 3 times with read pulse (+2 V, 0.64 ms) (**a**) when the pulse bit corresponding to "1" is one ([1000], [0100], [0010], [0001]), (**b**) when the pulse bit corresponding to "1" is two ([0101], [1010], [0011], [0110], [1100], [1001]), (**c**) when the pulse bit corresponding to "1" is three ([1101], [0111], [1011], [1110]), (**d**) when the pulse bit corresponding to "1" is zero ([0000]), and (**e**) when the pulse bit corresponding to "1" is four ([1111]).

Pulse Interval	+5Vx10	+5Vx20	+7Vx20
5s	4	3	
10s		1	2







Fig. S5. In the case of pulse condition 2, response of GDC/CeO₂ memristors by repeatedly applying a pulse train to a binary 4-bit input for a total of 3 times with read pulse (+2 V, 0.64 ms) (**a**) when the pulse bit corresponding to "1" is one ([1000], [0100], [0010], [0001]), (**b**) when the pulse bit corresponding to "1" is two ([0101], [1010], [0011], [0110], [1100], [1001]), (**c**) when the pulse bit corresponding to "1" is three ([1101], [0111], [1011], [1110]), (**d**) when the pulse bit corresponding to "1" is zero ([0000]), and (**e**) when the pulse bit corresponding to "1" is four ([1111]).

Pulse Interval	+5Vx10	+5Vx20	+7Vx20
5s	4	3	
10s		1	2







Fig. S6. In the case of pulse condition 3, response of GDC/CeO₂ memristors by repeatedly applying a pulse train to a binary 4-bit input for a total of 3 times with read pulse (+2 V, 0.64 ms) (**a**) when the pulse bit corresponding to "1" is one ([1000], [0100], [0010], [0001]), (**b**) when the pulse bit corresponding to "1" is two ([0101], [1010], [0011], [0110], [1100], [1001]), (**c**) when the pulse bit corresponding to "1" is three ([1101], [0111], [1011], [1110]), (**d**) when the pulse bit corresponding to "1" is zero ([0000]), and (**E**) when the pulse bit corresponding to "1" is four ([1111]).



Fig. S7. Recognition of handwritten digit images using a memristor-based RC system. (a) Confusion matrix with training data, (b) confusion matrix with test data, and (c) the simulation results of accuracy at the 15th epoch of 4-bit classification for RC system in the pulse conditions +7 V×20 read at +2V. (d) Confusion matrix with training data, (e) confusion matrix with test data, and (f) the simulation results of accuracy at the 15th epoch of 4-bit classification for RC system in the pulse conditions +5 V×20 read at +2V.



Fig. S8. Recognition of handwritten digit images using a memristor-based RC system. Confusion matrix with training data in conditions (a) +5 V×20 read at +2V, interval 10 s (condition 1), (b) linear case 1, and (c) linear case 2.