Electronic Supplementary Information

Logic Inverters Based on the Property Modulated Si Nanowires by Controlled Surface Modifications

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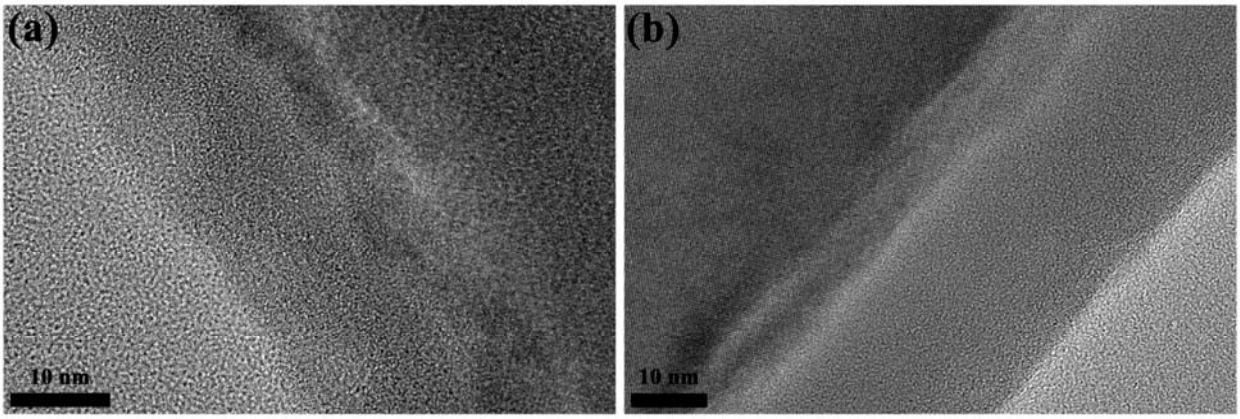

Figure S1. TEM images of heat treated *n*-type Si NWs for (a) 10 and (b) 20 min at 900 °C. The surface of Si NWs was oxidized to SiO_2 at the rate of 1.3 nm a minute. The surface of NW is smoother than as synthesized NW.

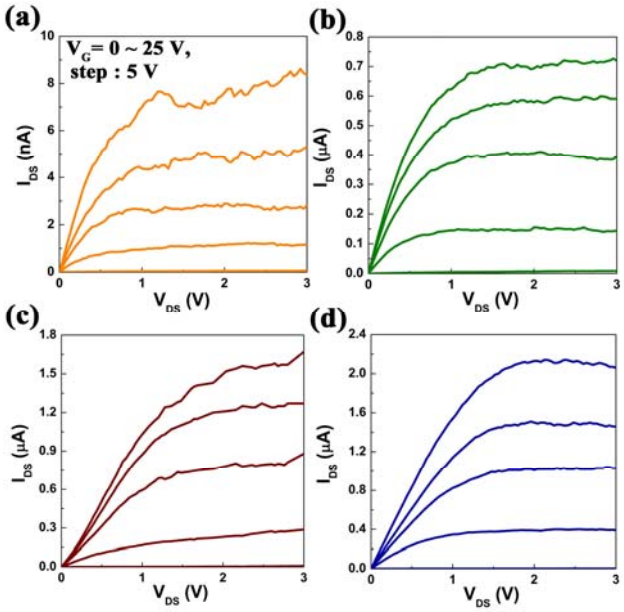

Figure S2. Output characteristics (I_{DS}– V_{DS}) of (a) as-synthesized *n*-type Si NWs and heat treated Si NWs for (b) 10, (c) 20, and (d) 30 min.

Table S3. The electrical properties in each state were represented by numerical table

	as-synthesized	**10 min**	**20 min**	**30 min**
Mobility (cm^2/Vs)	1 ~ 40	40 ~ 100	110 ~ 440	190 ~ 450
Subthreshold swing (V/decade)	1.4 ~ 4.0	1.4 ~ 2.1	1.4 ~ 2.3	1.3 ~ 2.1
Threshold voltage (V_{th})	–2 ~ 9	–3 ~ 5	–6 ~ 1	–12 ~ –5
Yield (%)	9	67	92	89

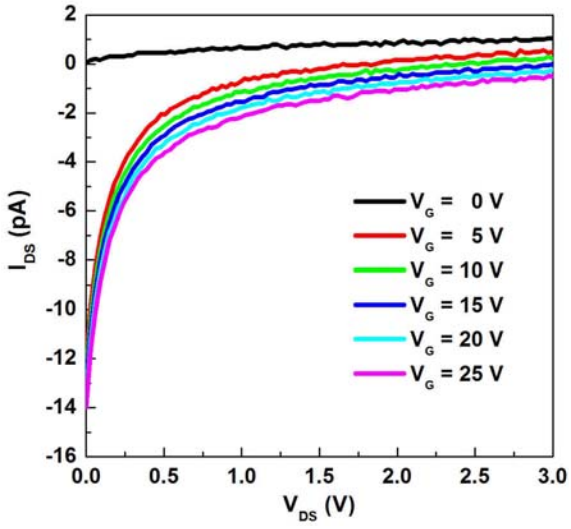

Figure S4. Typical I_{DS}– V_{DS} relations measured on a test structure prepared by depositing Ag and Au electrodes on cured PVP/SiO_2 without Si NWs.