Supporting Information for

Synergistically engineered self-standing silicon/carbon composite arrays as high performance lithium battery anodes

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Experimental Section

Synthesis of uniform, vertically aligned Si NWs: Silicon wafers (orientation 100, p-type 15-30 Ω cm) were used in this work. Uniform, vertically aligned Si nanowires (NWs) were synthesized by a colloidal mask-sustained metal-assisted chemical etching method following the literatures reported elsewhere.[1,2] In detail, a plasma oxygen exposure of the as-received silicon wafer was carried out to render their surface hydrophilic for the colloidal assembly. The colloidal self-assembly of polystyrene colloidal particles was performed carefully by spreading a diluted colloidal suspension at the water-air interface. After compaction, the film was transferred onto the plasma-treated wafer and dried in air. After reducing the particle size by an oxygen reactive ion etching approach, a 30 nm thick gold (Au) film was subsequently deposited by physical vapor deposition. The metal-assisted chemical etching was performed in an aqueous solution containing 4.8 M HF and 0.2 M H_2O_2 in ambient conditions under continuous agitation. The length of the Si nanowires was tuned by the etching time (e.g., ca. 2 h for 60 μm). After etching, the residual Au and

polystyrene particles were removed by the mixture of concentrated HCl and HNO_3 (v:v; 3:1) and toluene, respectively. The sample was let dry in air to get uniform, well-aligned Si NWs.

Preparation of wt-Si/C arrays: Firstly, the wafer with uniform, vertically aligned Si NWs was placed in a quartz boat, heated in air at a rate of 5 ℃ min^{-1} to 750 ℃ for a certain time to form SiO_2 layers on Si NWs. After that, the obtained sample was further coated with a carbon layer by applying a CVD process. In detail, the sample was heated to 1050 ℃ at a rate of 20 ℃ min^{-1} in a horizontal tube furnace under argon/hydrogen (Ar/H_2) (2:1) atmosphere, then 100 sccm CH_4 was introduced into the reaction tube and kept for 5 min. After the deposition, the furnace was rapidly cooled down to room temperature. Finally, the as-processed wafer was immersed in 5% HF solution to remove SiO_2 sacrificial layers to realize Si/C wire-in-tube nanocomposites with an array modality which was inherited from that of the original Si NWs.

Fabrication of free-standing wt-Si/C arrays: The silicon wafer with a wt-Si/C nanocomposite array was immersed into 5% NaOH aqueous solution to have the wt-Si/C array spontaneously delaminated from the wafer. During this process, the carbon tubes function as barriers to effectively hinder the etching of Si NWs by NaOH solution, while the pores at the bottom of the array formed during the metal-assisted chemical etching process promote the uptake and diffusion of NaOH solution and thus facilitate the delamination of the array from the wafer. The as-prepared array was further washed with deionized water copiously to remove any residues, dried in vacuum, thus completing the fabrication of a free-standing wt-Si/C array.

Characterizations: The morphology and structure of the samples were investigated by FE-SEM (Hitachi S4800) and FE-TEM (FEI Tecnai G2 20 STWIN and Tecnai G2 F20 U-TWIN). The X-ray diffraction (XRD) instrument type was D/MAX-TTRⅢ (CBO). Raman spectra were collected using a Renishaw inVia Raman microscope with a laser wavelength of 514.5 nm. For electrochemical measurements, the free-standing wt-Si/C arrays were directly used as the working electrode. As a control, the wt-Si/C (PVDF) electrodes were prepared by mixing the active material (wt-Si/C nanocomposites collected from the substrate) with Super-P carbon black and poly(vinylidene fluoride) (PVDF) binder in N-methyl-2-pyrrolidone (NMP) at a weight ratio of 80:10:10, and then casting on current collectors (copper foil). The materials weight of individual electrodes is typically 1.5-3.0 mg. The as-made working electrodes were assembled into coin-type half cells (CR2032) in an argon-filled glovebox (< 0.1 ppm of water and oxygen) with lithium foil as the counter electrode, porous polypropylene film as the separator, and 1M $LiPF_6$ in 1:1 (v/v) ethylene carbonate/diethyl carbonate (EC/DEC) as the electrolyte (no any additive used). The cycle-life test was performed using a CT2001A battery program controlling test system at different rates within the 2-0.02 V voltage range. Unless otherwise specified, all capacities in this work were based on the total mass of the active materials (wt-Si/C nanocomposites); in the case of wt-Si/C array electrodes, the total mass of the active materials corresponds to the electrode weight because of the absence of any additives. The areal capacities were calculated based on product of the specific capacity values and the active material mass loadings.

Figure S1-S12

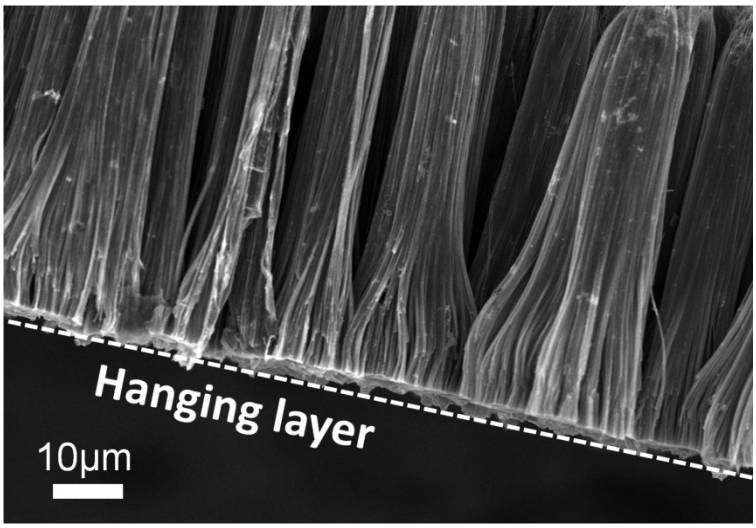

Figure S1. SEM image shows a thin hanging layer at the bottom of the array, which may originate from unfinished and interconnected Si domains created during the SiNW synthesis process.

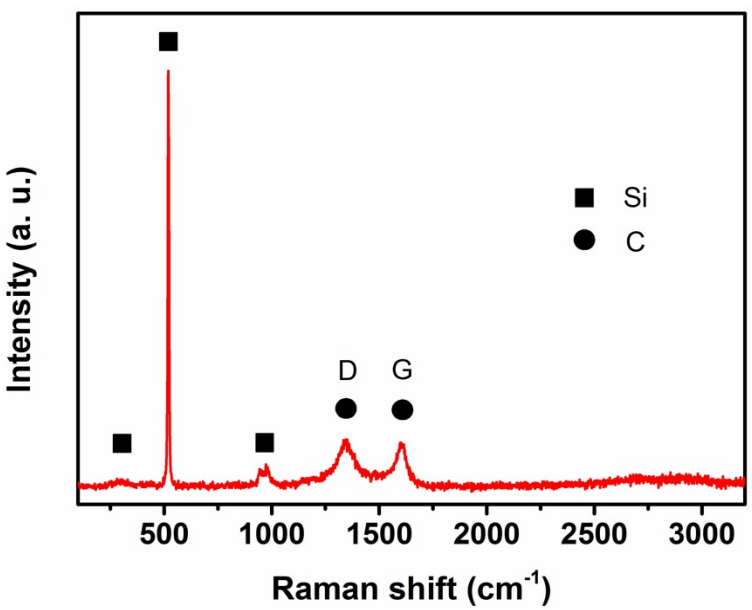

Figure S2. Raman spectrum of wt-Si/C array. In the spectrum, three peaks below 1000 cm^{-1} are ascribed to the crystalline Si NW cores. In addition, the two peaks appearing at about 1350 and 1590 cm^{-1} are assignable as the D band originating from disordered carbon, and G band corresponding to sp^2 compositeized carbon, respectively, both of which can originate from graphitic carbon.

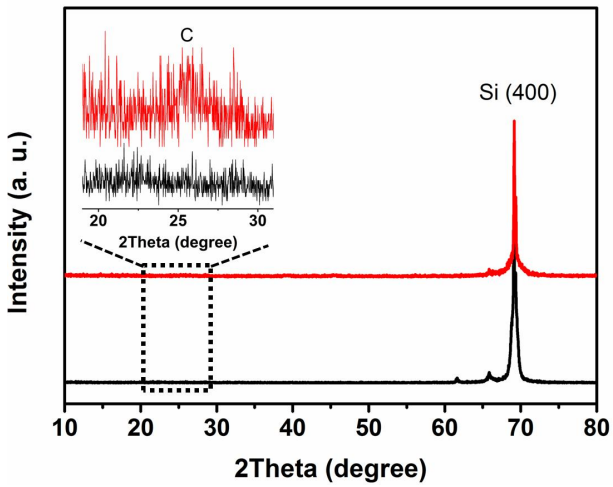

Figure S3. XRD patterns of (top) wt-Si/C array and (bottom) Si NWs. In both patterns an apparent peak appearing at 69° is fitting well to the (400) characteristic reflection of crystalline Si, consistent with the use of (100) silicon wafers in this work. Furthermore, in the enlarged view a peak at ca. 26° assigning to graphitic carbon can be observed in the pattern of the wt-Si/C array.

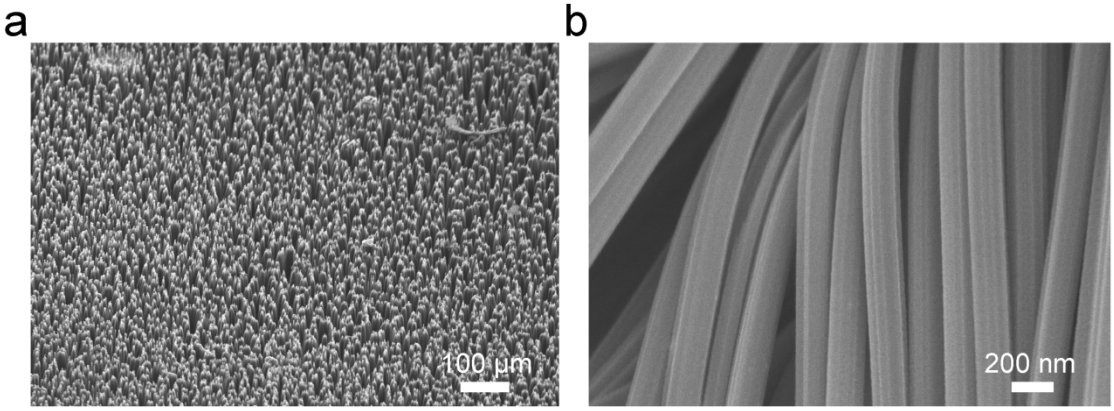

Figure S4. SEM images of uniform, well-aligned Si NWs.

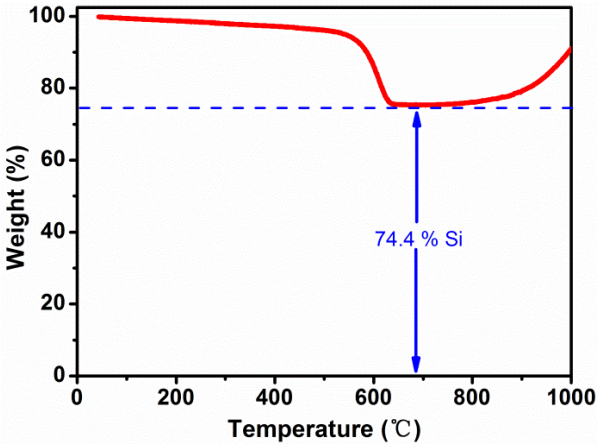

Figure S5. TGA profile of wt-Si/C array, showing ca. 74.4 wt% content of Si in the wt-Si/C array.

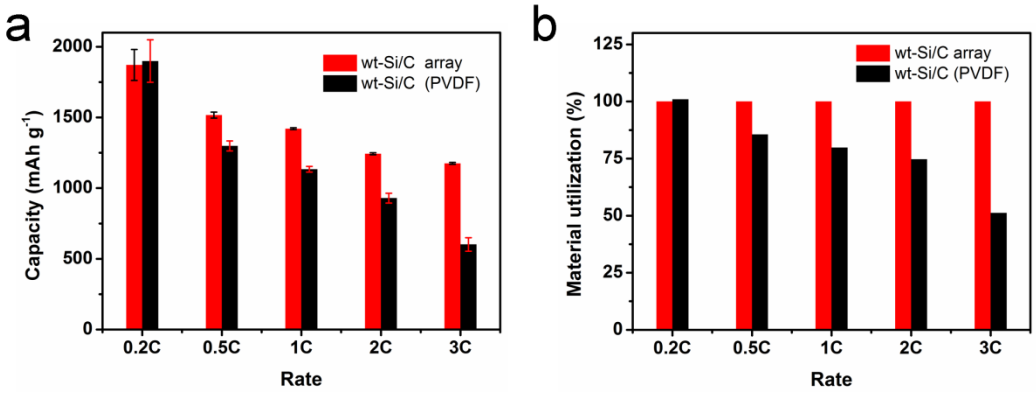

Figure S6. (a) Comparison of specific capacities of wt-Si/C array and wt-Si/C (PVDF) electrodes at various rates; (b) Relative material utilization degree of wt-Si/C array anode in comparison with that of wt-Si/C (PVDF) anode. Note: materials utilization denotes the lithium storage capability of silicon.

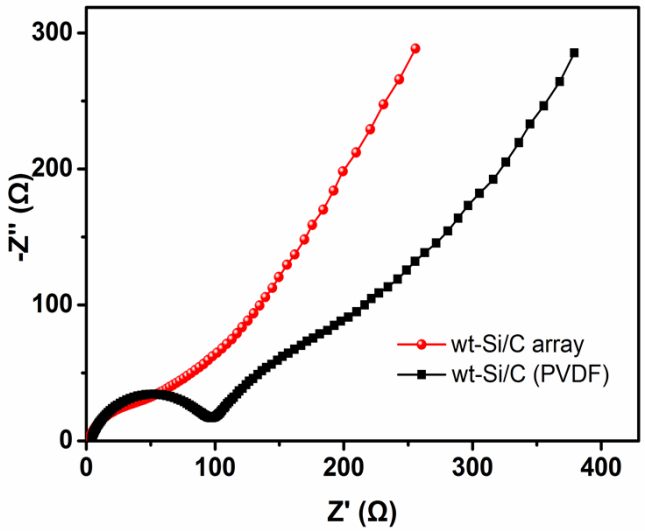

Figure S7. Electrochemical impedance spectroscopy (EIS) spectra of wt-Si/C array anode in comparison with that of wt-Si/C (PVDF) anode. Both EIS spectra comprise a depressed semicircle in the high-frequency region corresponding to interfacial charge transfer impedance, and an inclined line in the low-frequency region reflecting solid-state diffusion of lithium ions. The comparison of the semicircle diameters clearly discloses that the charge transfer resistance of wt-Si/C array is significantly smaller than that for wt-Si/C (PVDF) anode, which reflects fast electron transport in the wt-Si/C array. On the other hand, a steeper slope of the inclined line for wt-Si/C array anode compared with that for wt-Si/C (PVDF) anode is observed at the low-frequency region, depicting the efficiency of vertical channels (that is, void spaces in between wt-Si/C nanocomposites) in the array for fast diffusion and transport of lithium ions.

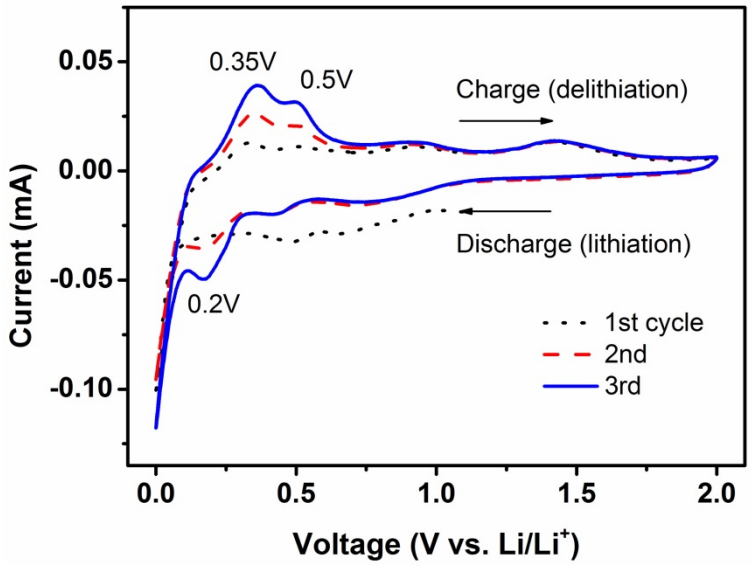

Figure S8. Typical cyclic voltammetry (CV) curves of wt-Si/C array measured at the current rate of 0.1 mV s^{-1}. The distinct peaks appeared at 0.2V during discharge and at 0.35 and 0.5V during charge represent the characteristic phase transformation between amorphous Si and Li_xSi. Note: the peaks near 0.9 V and 1.5 V may be related to the presence of carbon tubes, of which partially reversible reactions with lithium ions occur.[3,4]

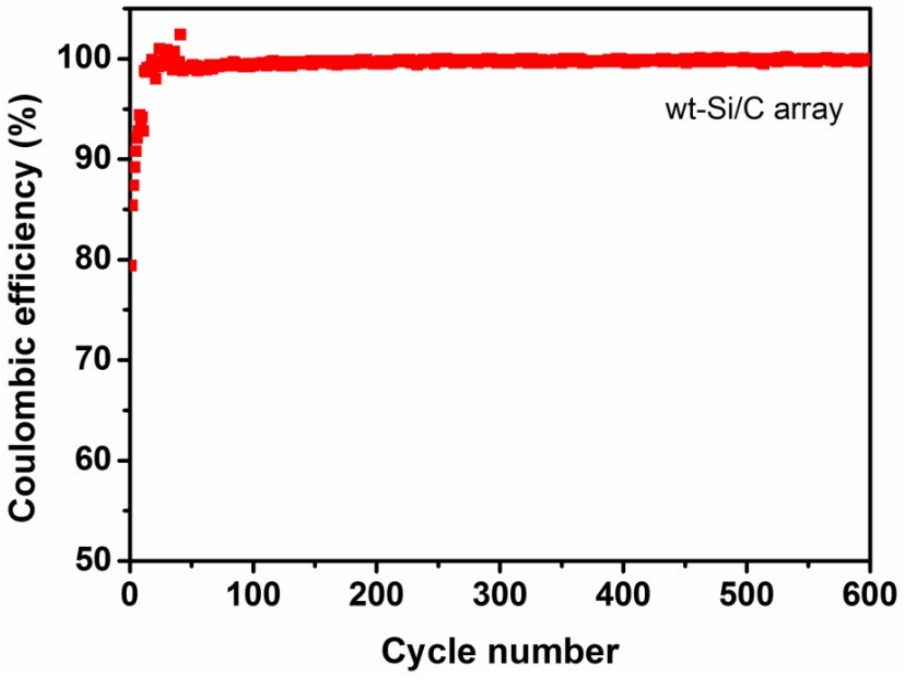

Figure S9. Coulombic efficiency plot of wt-Si/C array cycled between 0.02 and 2V. The Coulombic efficiency increases gradually to 94% at the 10th cycle, and then fluctuates around 99% from the 11st and 41st cycles. From the 42nd cycle, the Coulombic efficiency stabilizes at 99.7%.

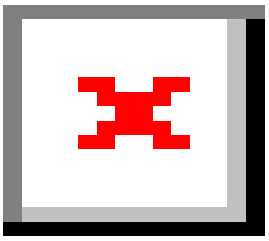

Figure S10. Electrochemical impedance spectroscopy (EIS) spectrum of the wt-Si/C array anode tested after 600 cycles with the original one superimposed. The profile preservation indicates the structural and interfacial stability of such designed electrode structures.

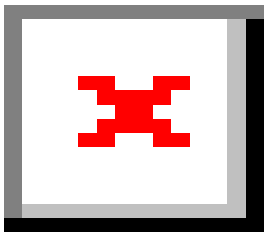

Figure S11. The first-cycle voltage profiles for wt-Si/C array.

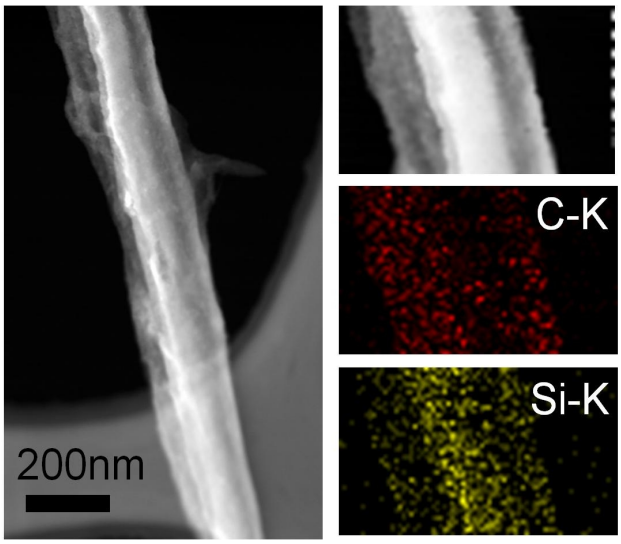

Figure S12. TEM image and elemental mapping (carbon and silicon) of an individual nanocomposite of the wt-Si/C array after long-term cycling.

References

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